

VDS	RDS(on)	ID@25℃
1200V	75mΩ	33A

Applications:

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC Converters
- EV Charging
- Motor Drives

Features:

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness

Benefits:

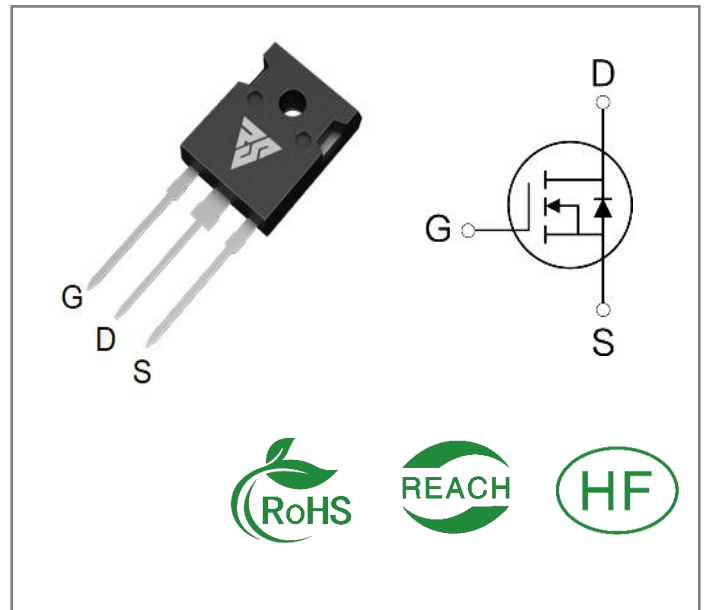
- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSM120075W	TO-247-3	RSM120075W	Tube	30 PCS

Maximum Ratings (TJ= 25℃ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
VDSmax	Drain - Source Voltage	1200	V	VGS=0V, ID =100μA	
VGSmax	Gate - Source Voltage	-8/+22	V	Absolute maximum values	
VGSop	Gate - Source Voltage	-4/+18	V	Recommended operational values	
ID	Continuous Drain Current	33 23.8	A	VGS=18V, TC =25℃ VGS=18V, TC =100℃	
ID(pulse)	Pulsed Drain Current	80	A	Pulse width tp limited by TJmax	
PD	Power Dissipation	136	W	TC =25℃, TJ =175℃	
TL	Solder Temperature	260	℃		
TJ, Tstg	Operating Junction and Storage Temperature	-55 to +175	℃		



Electrical Characteristics (T_J= 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V(BR)D SS	Drain-Source Breakdown Voltage	120 0			V	V _{GS} =0V, I _D =100μA	
V _{GS} (th)	Gate Threshold Voltage	1.9	2.6	4.0	V	V _{GS} = V _{DS} , I _{DS} =5mA, TC =25°C	
			1.8		V	V _{GS} = V _{DS} , I _{DS} =5mA, TC =175°C	
I _{DSS}	Zero Gate Voltage Drain Current		1	100	μA	V _{DS} = 1200V, V _{GS} =0V	
I _{GSS} +	Gate-Source Leakage Current		10	250	nA	V _{GS} =22V, V _{DS} = 0V	
I _{GSS} -	Gate-Source Leakage Current		10	250	nA	V _{GS} =-8V, V _{DS} = 0V	
R _{DS} (on)	Drain-Source on-state Resistance		75	95	mΩ	V _{GS} =18V, I _D =20A, TC =25°C	
			120			V _{GS} =18V, I _D =20A, TC =175°C	
C _{iss}	Input Capacitance		120 0		pF	V _{GS} =0V, V _{DS} =1000 V, f=1MHz, V _{AC} =25 mV	
C _{oss}	Output Capacitance		63				
C _{rss}	Reverse Transfer Capacitance		9.8				
E _{ON}	Turn-On Switching Energy		586		μJ	V _{DS} =800V, V _{GS} =-4/18V, I _D = 20A, R _G (ext) = 2.5Ω, L= 100μH	
E _{OFF}	Turn-Off Energy		273				
t _d (on)	Turn-On Delay Time		13		ns	V _{DS} =800V, V _{GS} =-4/18 V I _D = 20A, R _G (ext) =2. 5 Ω , R _L =20Ω	
t _r	Rise Time		12				
t _d (off)	Turn-Off Delay Time		16				
t _f	Fall Time		10				
R _G (int)	Internal Gate Resistance		5.5		Ω	f=1 MHz, V _{AC} =25mV	
Q _{gs}	Gate to Source Charge		21.5		nC	V _{DS} =800V, V _{GS} =-4/18V I _D =20A	
Q _{gd}	Gate to Drain Charge		14.6		nC		
Q _g	Total Gate Charge		68.1				

Reverse Diode Characteristics (T_J= 25°C unless otherwise specified)

Symbol	Parameter	Typ.	Max	Unit	Test Conditions	Note
VSD	Diode Forward Voltage	4.2		V	VGS=-4V, ISD =10 A, T _J = 25°C	
		3.8		V	VGS=-4V, ISD=10 A, T _J = 175°C	
IS	Continuous Diode Forward Current		33	A	VGS=-4V, TC= 25°C	
trr	Reverse Recovery time	28		ns	ISD= 20A, VR = 800V	
Qrr	Reverse Recovery Charge	62		nC		
Irrm	Peak Reverse Recovery Current	3.7		A		

Thermal Characteristics (T_J= 25°C unless otherwise specified)

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
R _{θJC}	Thermal Resistance from Junction to Case	0.84	°C/W		
R _{θJA}	Thermal Resistance From Junction to Ambient	40			

Typical Feature Curve

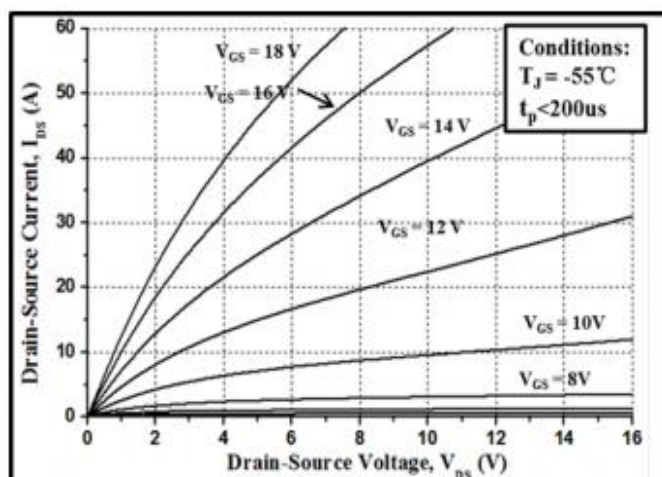


Figure 1. Output Characteristics $T_j = -55^\circ\text{C}$

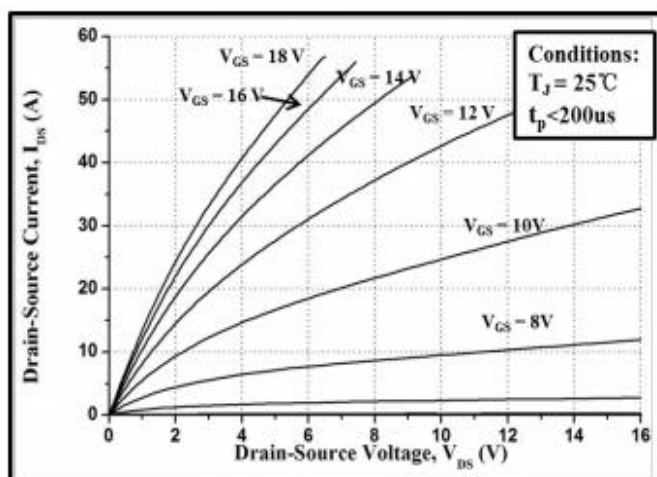


Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$

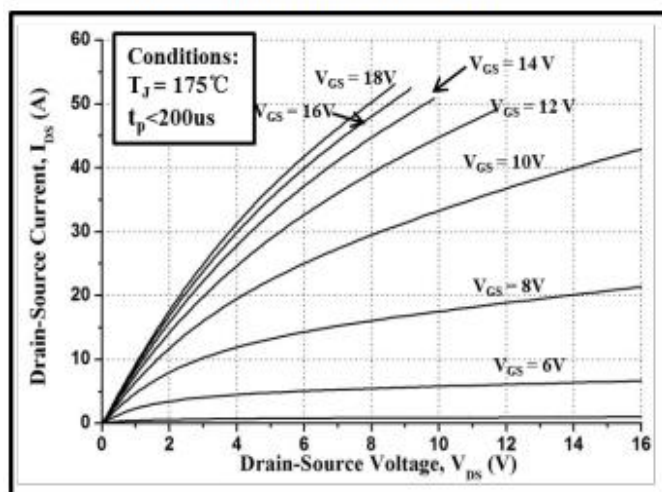


Figure 3. Output Characteristics $T_j = 175^\circ\text{C}$

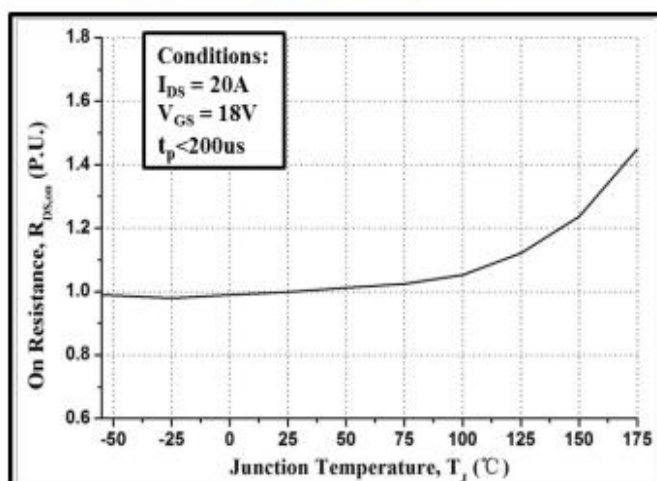


Figure 4. Normalized On-Resistance vs. Temperature

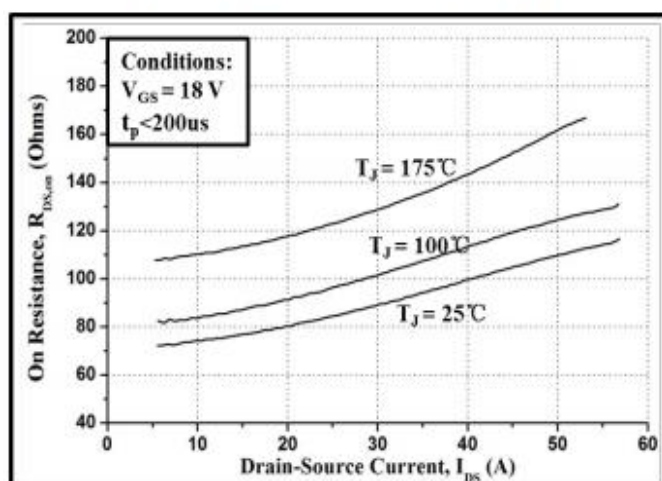


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

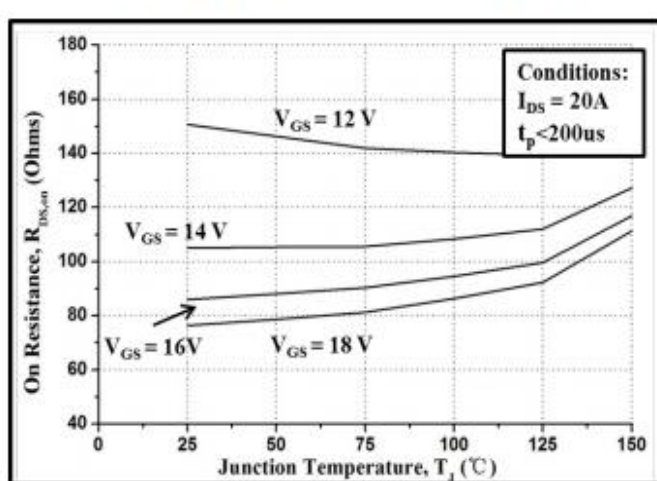


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

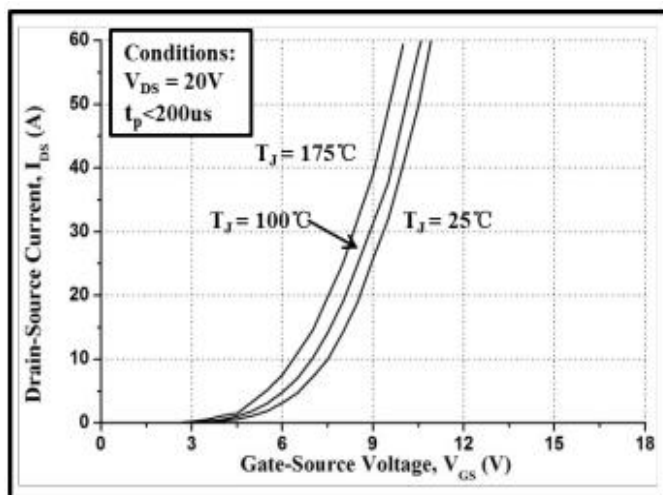


Figure 7. Transfer Characteristic for Various Junction Temperatures

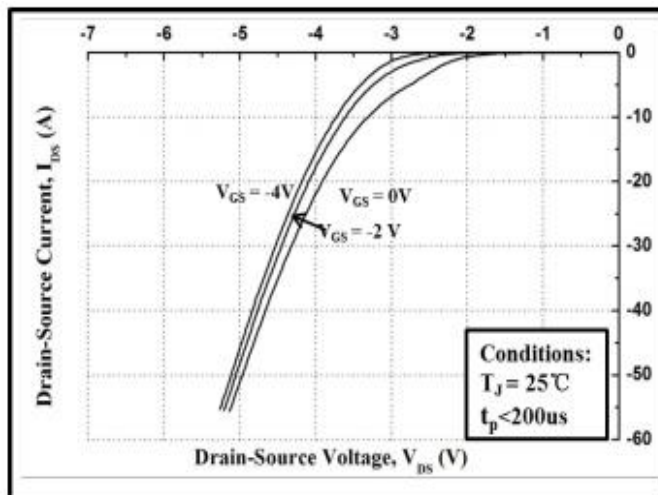


Figure 8. Body Diode Characteristic at 25°C

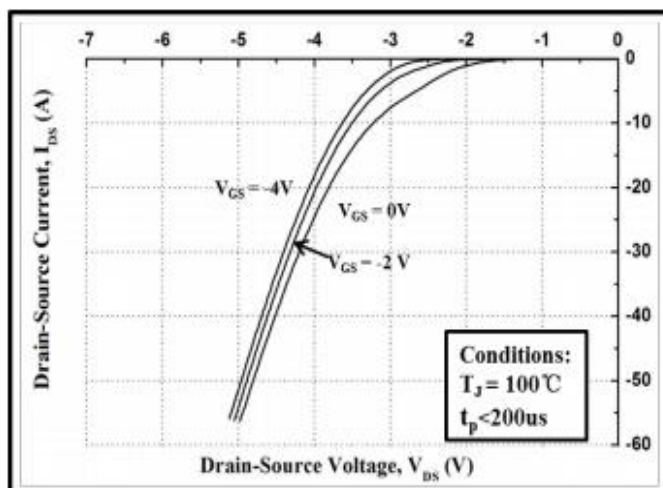


Figure 9. Body Diode Characteristic at 100°C

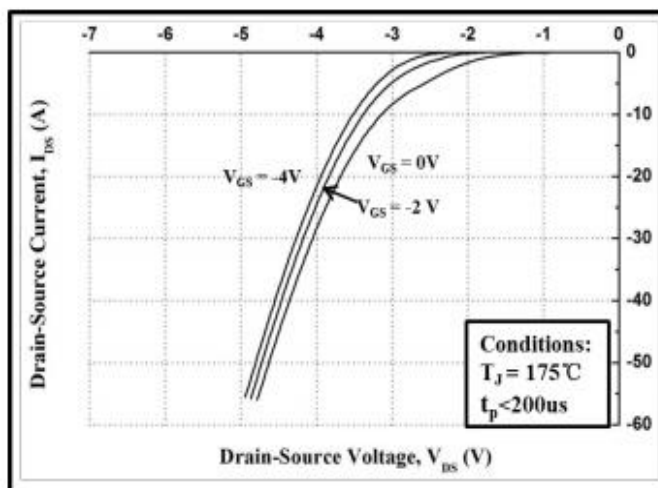


Figure 10. Body Diode Characteristic at 175°C

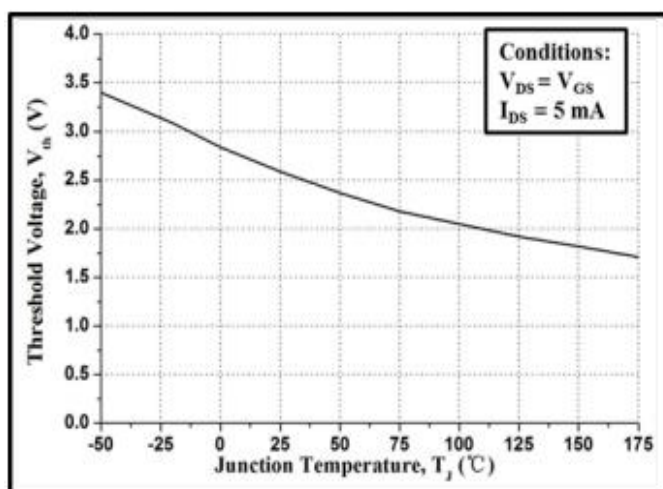


Figure 11. Threshold Voltage vs. Temperature

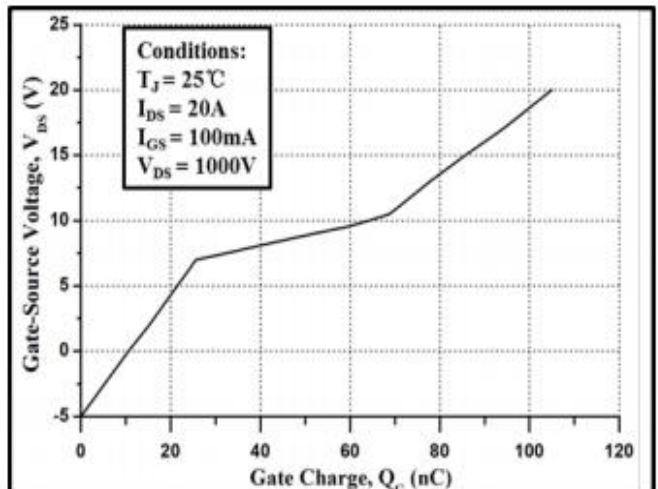


Figure 12. Gate Charge Characteristics

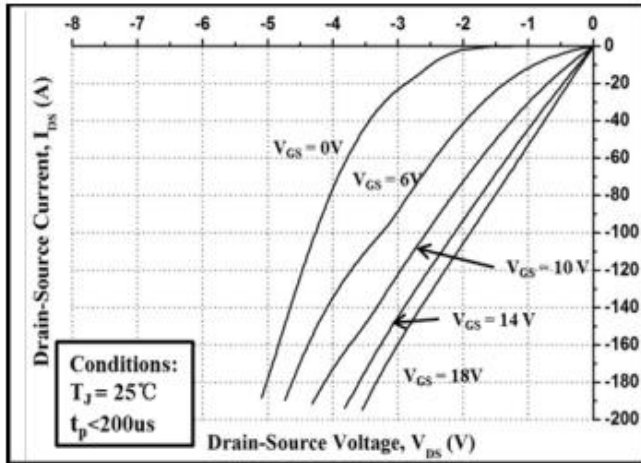


Figure 13. 3rd Quadrant Characteristic at 25°C

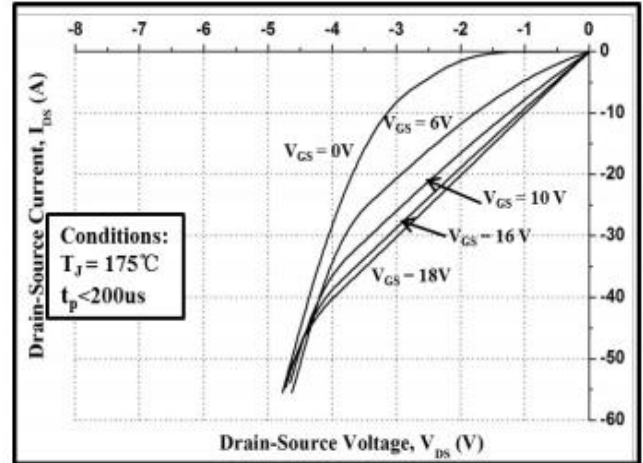


Figure 14. 3rd Quadrant Characteristic at 175°C

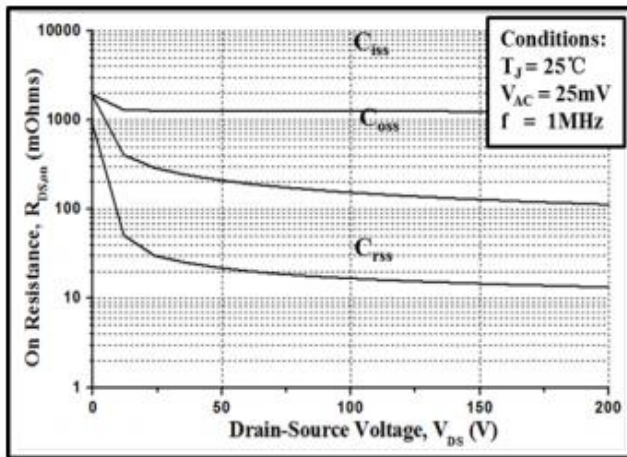


Figure 15. Capacitances vs. Drain-Source Voltage (0 - 200V)

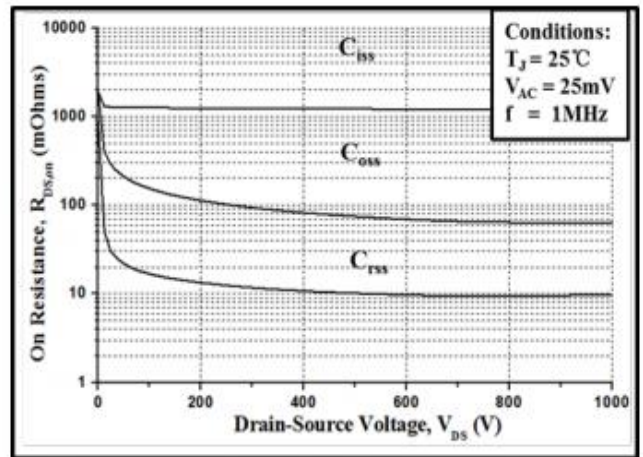
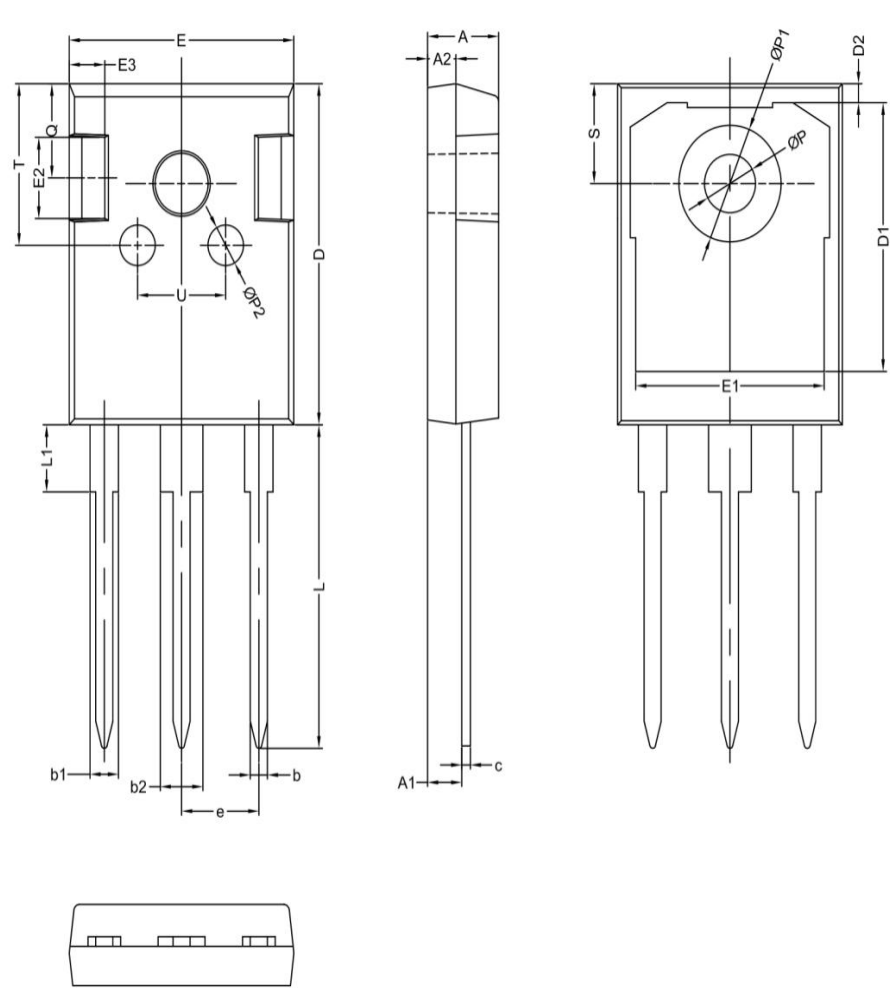


Figure 16. Capacitances vs. Drain-Source Voltage (0 - 1000V)

Package outline drawing(TO-247-3 Unit: mm)



符号	机械尺寸/mm		
	最小值	典型值	最大值
A	4.80	5.00	5.20
A1	2.21	2.41	2.61
A2	1.90	2.00	2.10
b	1.10	1.20	1.35
b1		2.00	
b2		3.00	
c	0.55	0.60	0.75
D	20.80	21.00	21.20
D1		16.55	
D2		1.20	
E	15.60	15.80	16.0
E1		13.30	
E2		5.00	
E3		2.50	
e		5.44	
L	19.42	19.92	20.42
L1		4.13	
P	3.50	3.60	3.70
P1	-	-	7.40
P2		2.50	
Q		5.80	
S	6.05	6.15	6.25
T		10.00	
U		6.20	

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