

ID	$R_{DS(ON)}$ (Typ)	VDSS
7A	1.1 Ω	500V

Applications:

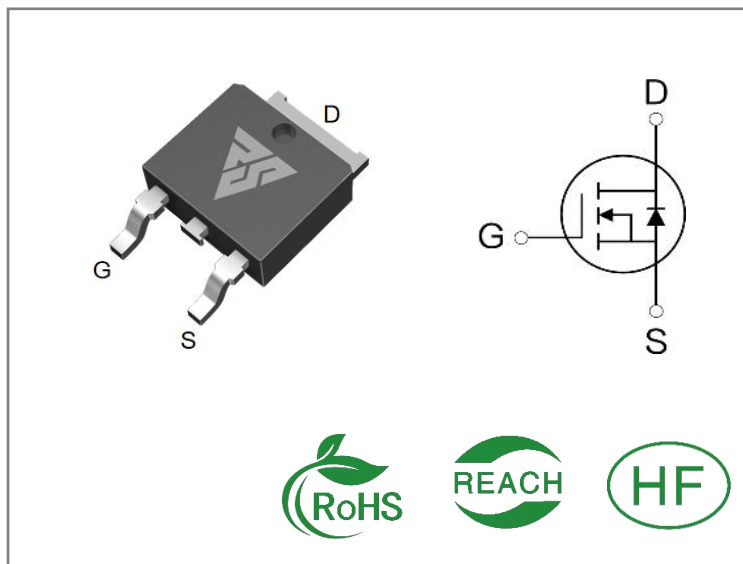
- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability
- Fast Recovery Time

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSF7N50D	T0-252	RSF7N50D	Tape&reel	2500 PCS



Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	RSF7N50D	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current $T_C = 25^\circ\text{C}$	7	A
IDM	Pulsed Drain Current (Note*1)	28	
PD	Power Dissipation	99	W
VGS	Gate- to- Source Voltage	± 30	V
EAS	Single Pulse Avalanche Energy $L = 10\text{mH}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, $T_C = 25^\circ\text{C}$	240	mJ
TL TPKG	Maximum Temperature for Soldering	300	$^\circ\text{C}$
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RSF7N50D	Units	Test Conditions
R θ JC	Junction-to-Case	1.58	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\text{C}$
R θ JA	Junction-to- Ambient	100		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25 $^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500	--	--	V	VGS=0V,ID=250 μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=500V,VGS=0 V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V ,VDS=0 V

ON Characteristics TJ=25 $^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	1.1	1.5	Ω	VGS=10V,ID=3.5A
VGS(TH)	Gate Threshold Voltage	3	--	4	V	VGS=VDS,ID=250 μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	35	--	nS	VDS=250V ID=7A RG=25 Ω
trise	Rise Time	--	7	--		
td(OFF)	Turn- OFF Delay Time	--	76	--		
tfall	Fall Time	--	29	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	680	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	73	--		
Crss	Reverse Transfer Capacitance	--	7.2	--		
Qg	Total Gate Charge	--	20	--	nC	VDS=400V ID=7A VGS=10V
Qgs	Gate- to- Source Charge	--	3	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	10	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	7	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	28	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=3.5A,VGS=0V
trr	Reverse Recovery Time	--	100	--	nS	VR=250V IS=3.5A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	0.23	--	μC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

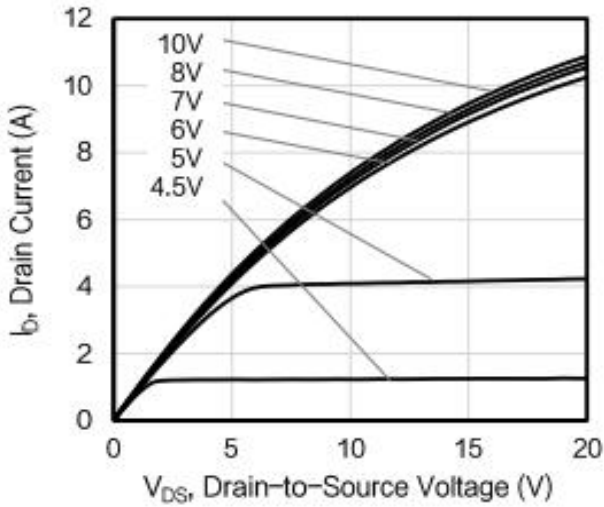


Figure 2. Body Diode Forward Voltage

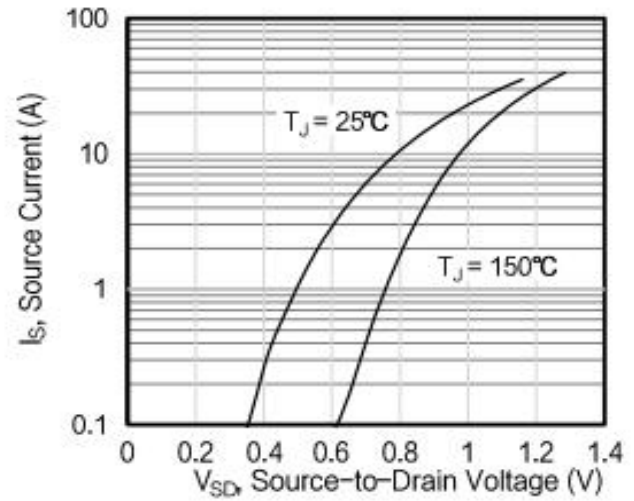


Figure 3. Drain Current vs. Temperature

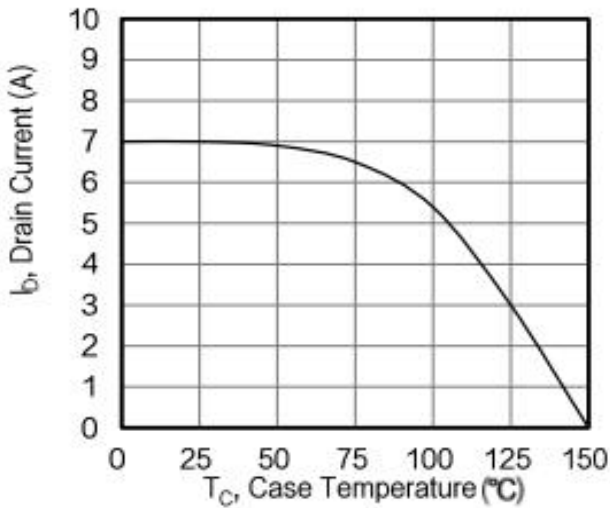


Figure 4. BV_{DSS} Variation vs. Temperature

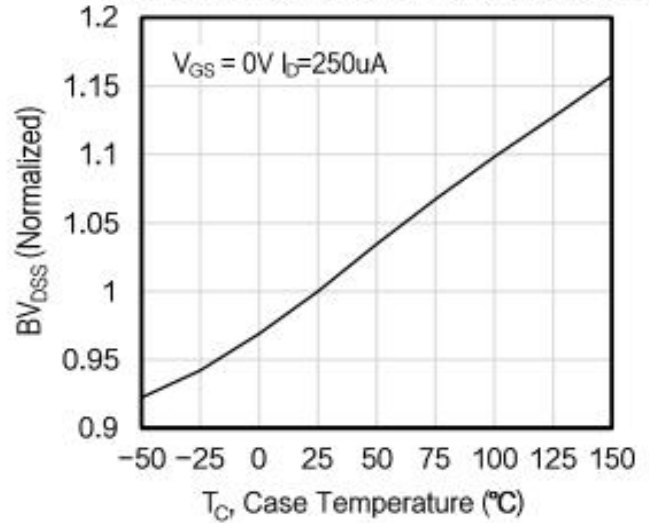


Figure 5. Transfer Characteristics

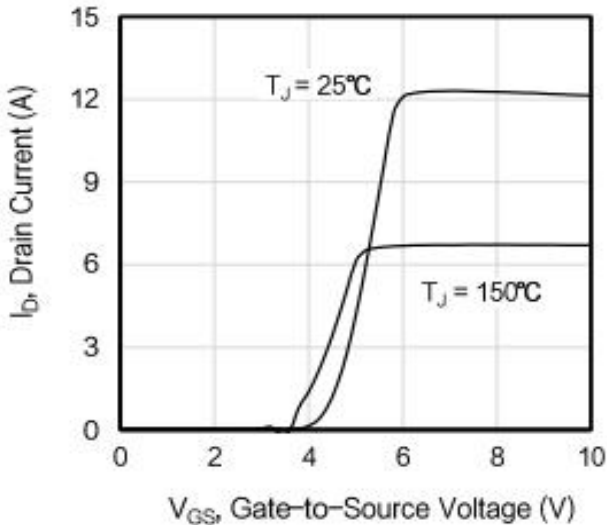


Figure 6. On-Resistance vs. Temperature

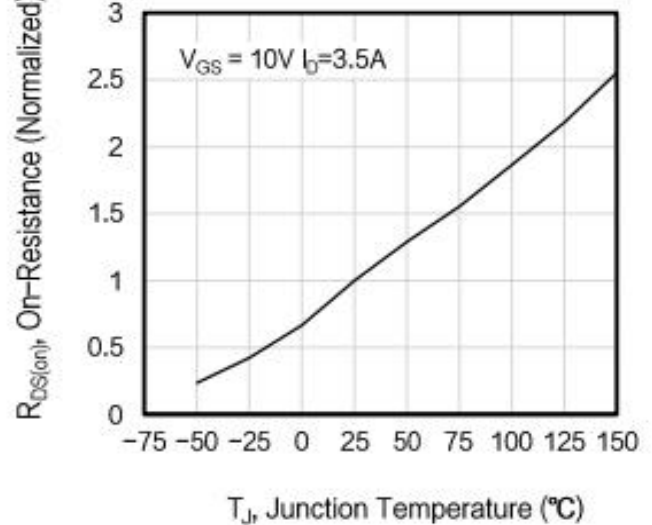


Figure 7. Capacitance

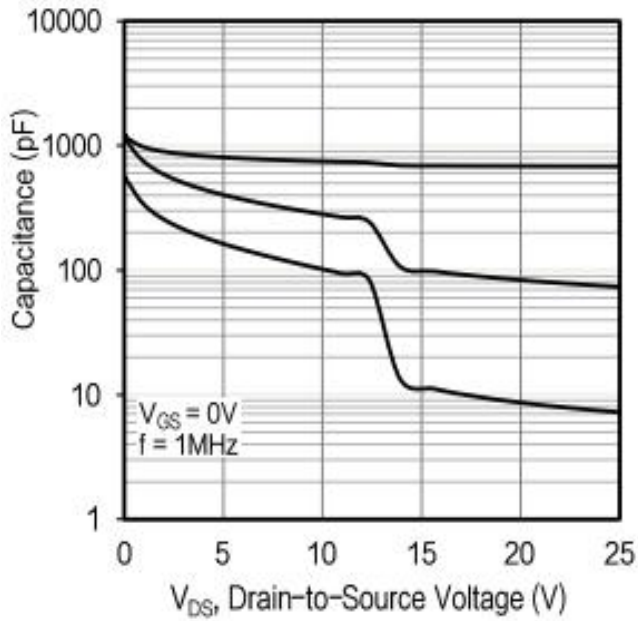


Figure 8. Gate Charge

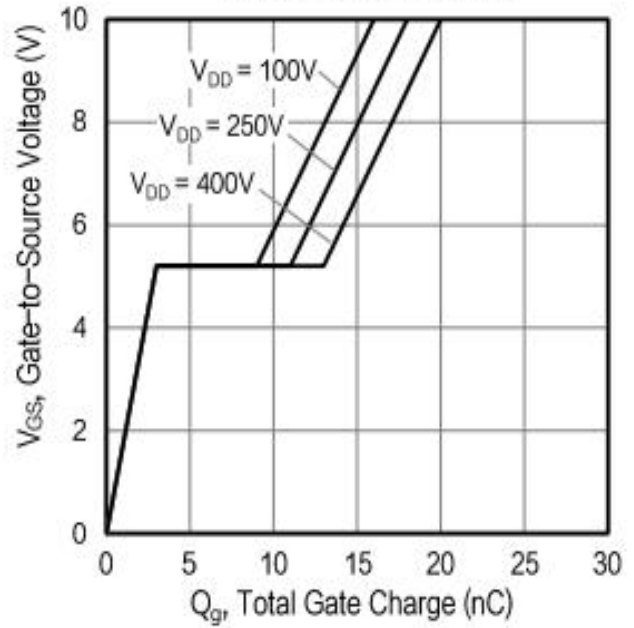


Figure 9. Transient Thermal Impedance

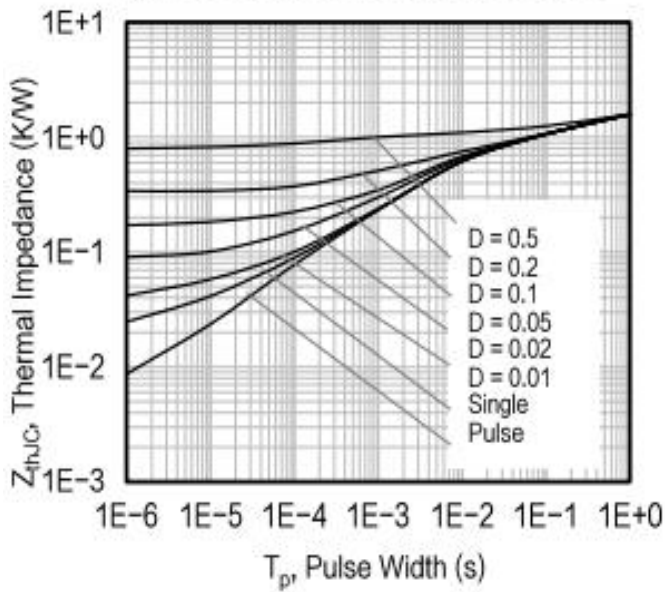
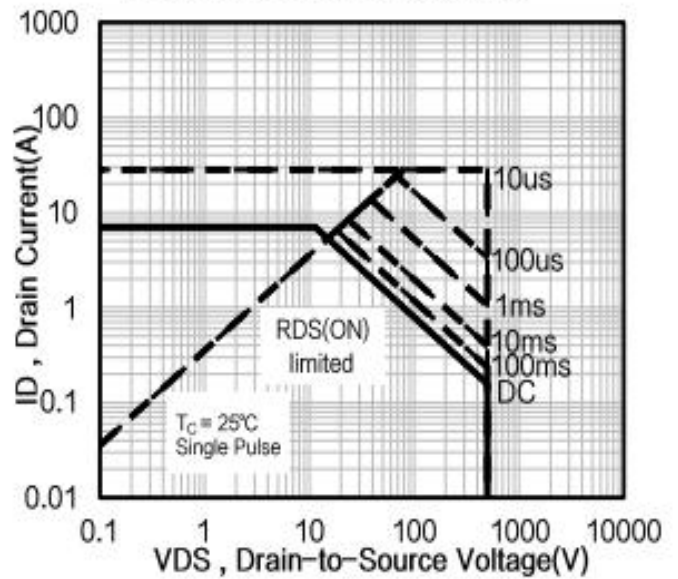


Figure 10. Safe Operating Area



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

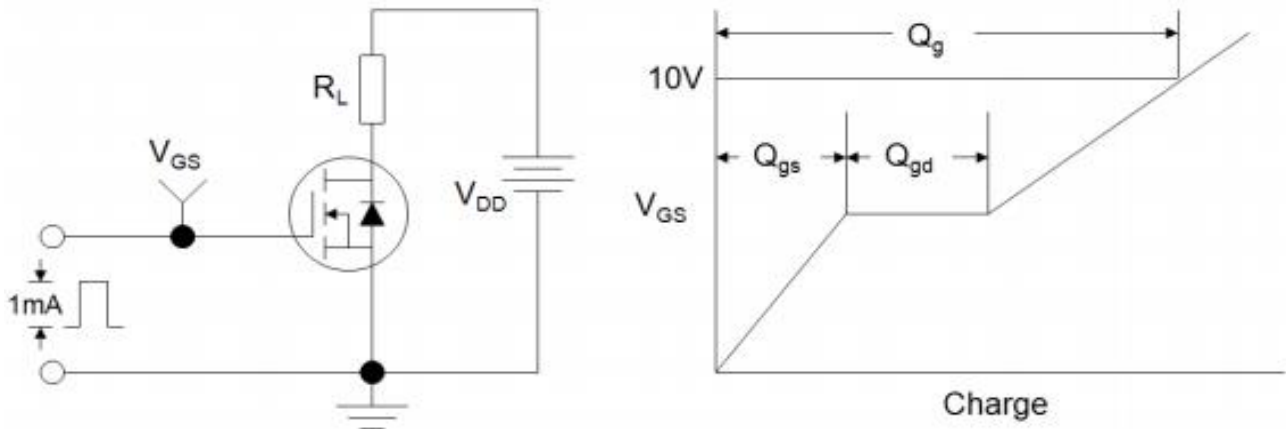


Figure B: Resistive Switching Test Circuit and Waveform

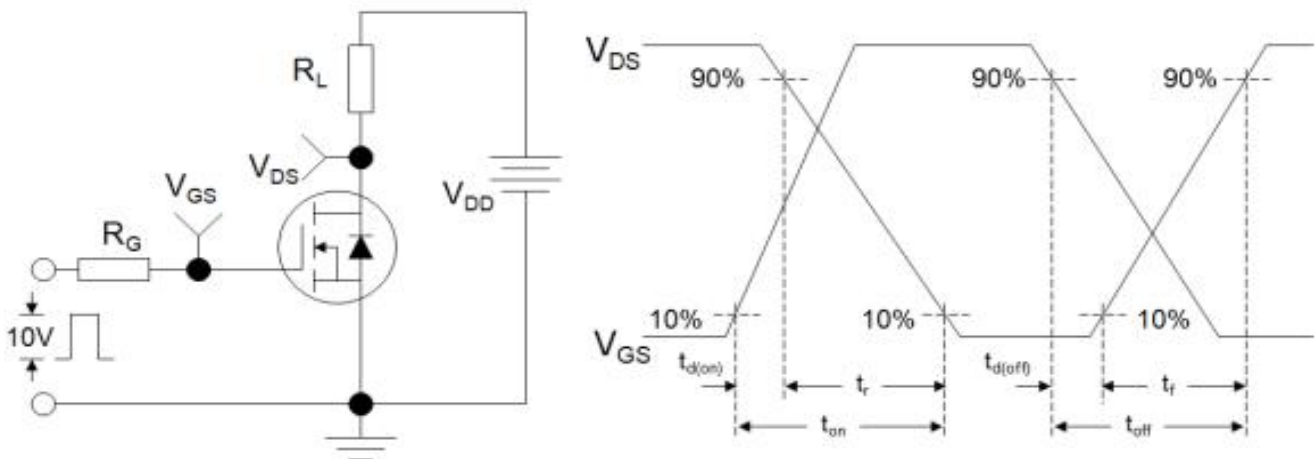
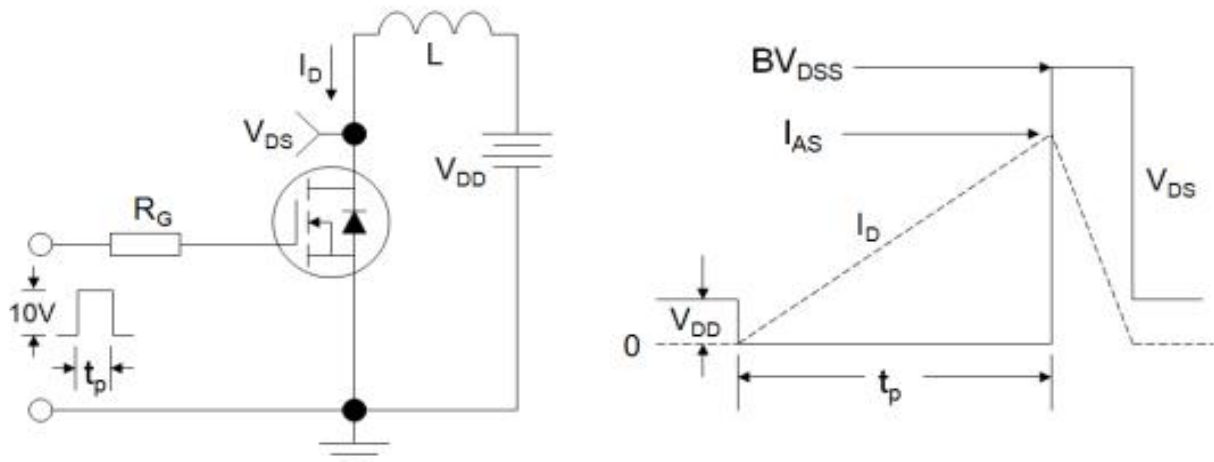
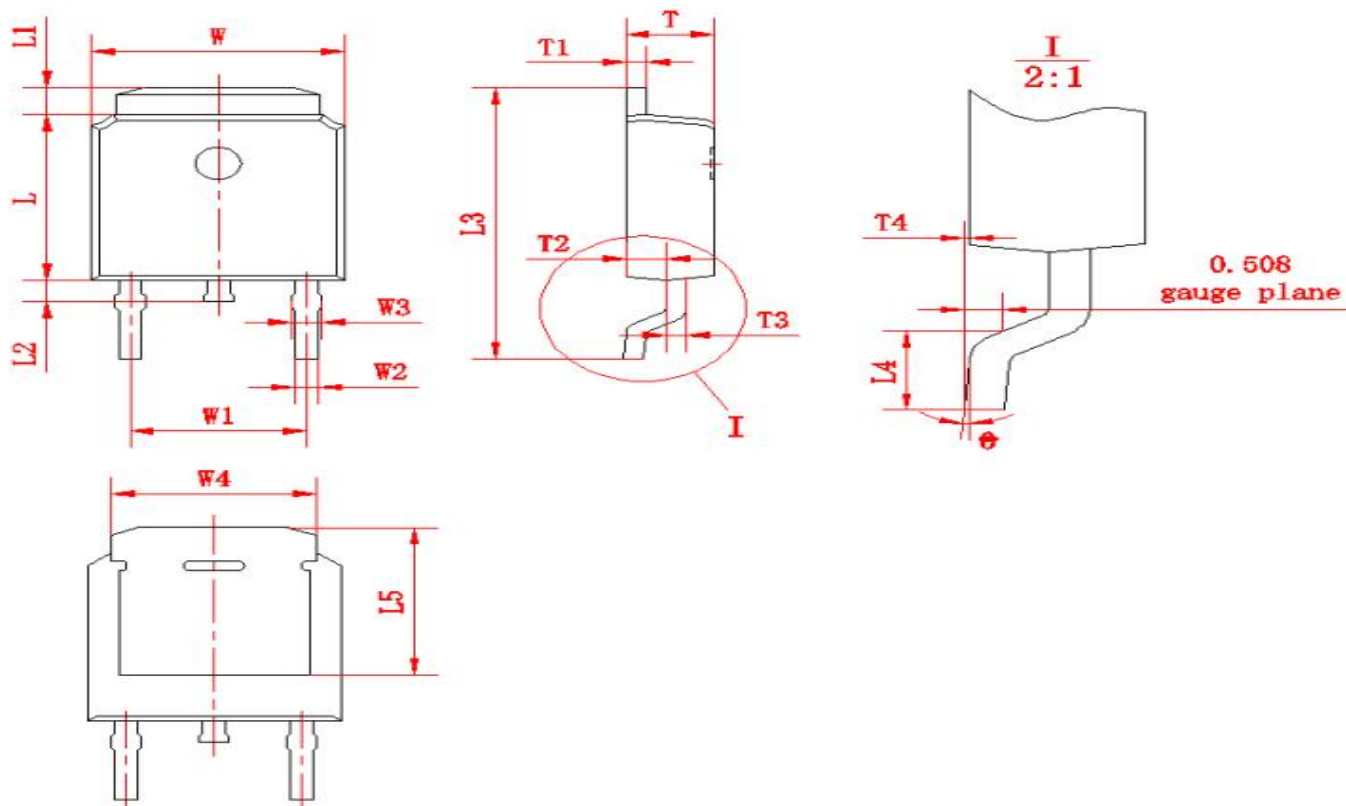


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing(TO-252 Unit: mm)


符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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