

VRRM	IF (TC≤135℃)	QC
1200V	36A	104nC

Applications:

- Switch Mode Power Supplies
- Power Factor Correction
- Motor drive, PV Inverter, Wind Power Station

Features:

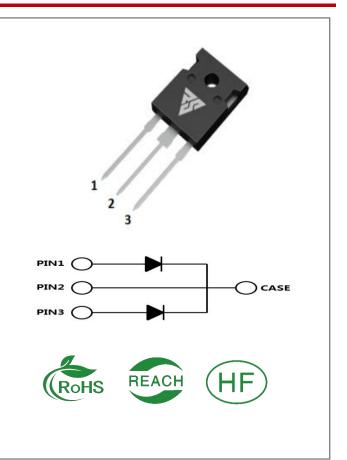
- Zero Reverse Recovery Current
- Zero Forward Recovery Voltage
- Positive Temperature Coefficient on VF
- Temperature-independent Switching
- 175°C Operating Junction Temperature

Benefits:

- Replace Bipolar with Unipolar Device
- Reduction of Heat Sink Size
- Parallel Devices Without Thermal Runaway
- Essentially No Switching Losses

Ordering	Information
Ordering	, mormation

Part Number	Part Number Package		Packing	Qty.	
RSS20120K	TO-247-3	RSS20120K	Tube	30 PCS	





Maximum Ratings (TJ= 25° C unless otherwise specified)

Symbol	Parameter	Value	Uni t	Test Conditions	Note
VRRM	Repetitive Peak Reverse Voltage	1200	V	TC = 25 ℃	
VRSM	Surge Peak Reverse Voltage	1200	V	TC = 25℃	
VR	DC Blocking Voltage	1200	V	TC = 25℃	
IF	Forward Current	36*21 8*210 /20	А	TC ≤ 25 ℃ TC ≤ 135 ℃ TC ≤ 159 ℃	Fig.3
IFSM	Non-Repetitive Forward Surge Current	60*24 5*2	A	TC = 25℃, tp = 10ms, Half Sine Wave TC = 110℃, tp = 10ms, Half Sine Wave	
IFRM	Repetitive Peak Forward Surge Current	55*2	А	TC = 25° C, tp = 10ms, Half Sine Wave	
Ptot	Power Dissipation	204*2	W	TC = 25℃	Fig.4
ТС	Maximum Case Temperature	159	°C		
TJ,TST G	Operating Junction and Storage Temperature	-55 to175	°C		

Electrical Characteristics (TJ= 25° C unless otherwise specified)

Symbol	Parameter	Тур.	Max.	Unit	Test Conditions	Note
VF	Forward Voltage	1.43 2.0	1.7 -	V	IF = 10A, TJ = 25℃ IF = 10A, TJ = 175℃	Fig.1
IR	Reverse Current	2 4	60 -	μΑ	VR = 1200V, TJ = 25℃ VR = 1200V, TJ = 175℃	Fig.2
С	Total Capacitance	110 0 92 78	/	pF	VR = 1V, TJ = 25°C, f = 1MHz VR = 400V, TJ = 25°C, f = 1MHz VR = 800V, TJ = 25°C, f = 1MHz	Fig.5
QC	Total Capacitive Charge	52	/	nC	VR =800V,	Fig.6
Ec	Capacitance Stored Energy	15.8		uJ	VR =800V,	Fig.7

Thermal Characteristics (TJ= 25°C unless otherwise specified)

Symbol	Parameter	Тур.	Unit	Note
RθJC	Thermal Resistance from Junction to Case	0.736	°C/W	Fig.8



Typical Feature Curve

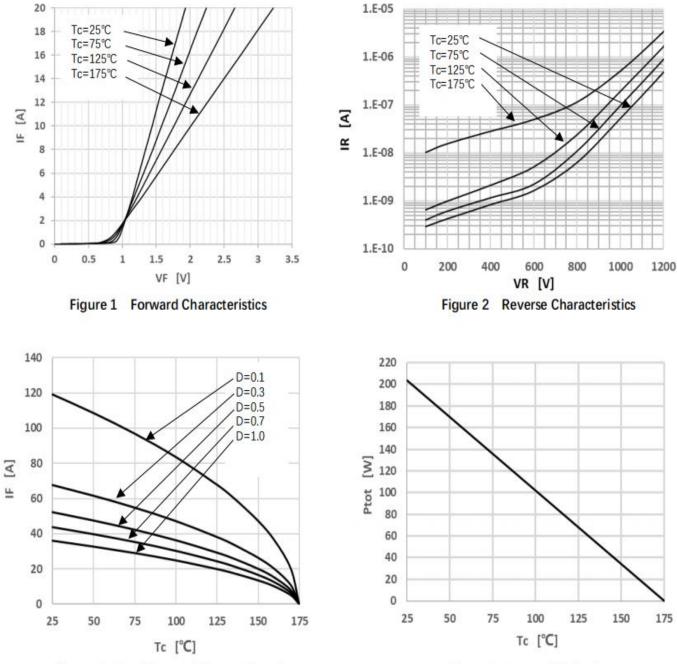
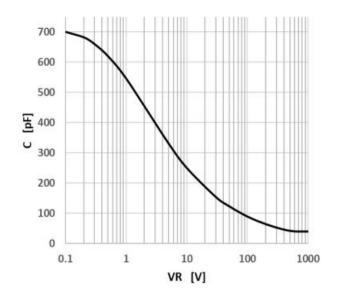
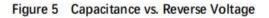


Figure 3 Peak Forward Current Derating

Figure 4 Power Dissipation







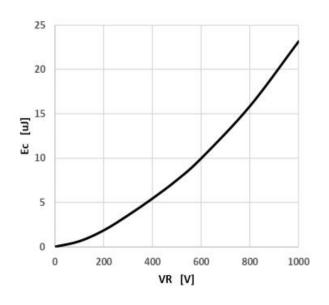


Figure 7 Capacitance Stored Energy

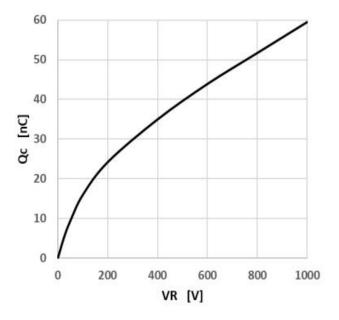


Figure 6 Capacitance Charge vs. Reverse Voltage

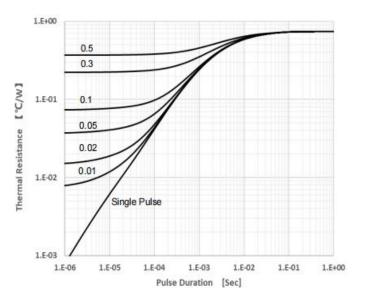
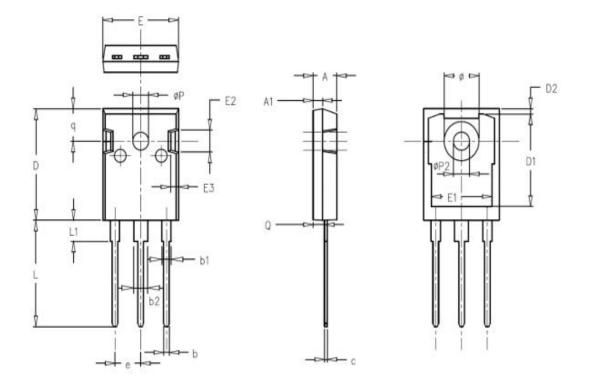


Figure 8 Transient Thermal Impedance



Package outline drawing(TO-247-3 Unit: mm)



SYMBOL	MILLIMETERS	NOTE	CANDOL	MILLIMETERS			NOT		
	N ormal	MIN.	MAX.	N OTES	SYMBOL	Normal	MIN.	MAX.	N OTES
A	4.98	4.68	5.36		øP	3.66	3.45	3.85	
A 1	1.99	1.90	2.10		e	5.44	BSC	BSC	
Q	2.41	2.30	2.60		q	6.24	5.99	6.58	
с	0.60	0.48	0.72		ØP2	3.45	3.24	3.64	
b	1.20	1.00	1.40		ø	7.14	7.10	7.30	
b1	2.07	1.90	2.30		D1	16.56	16.10	17.10	
b2	3.07	2.90	3.30		D2	0.98	0.80	1.36	
D	21.10	20.80	21.80		E1	13.30	13.00	13.52	1
E	15.98	15.38	16.20		E2	5.64	5.10	6.10	
L	20.28	19.50	20.50		E3	2.33	1.90	2.70	
L1	4.01	3.75	4.35			· · · · · · · · · · · · · · · · · · ·			



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