

ID	$R_{DS(ON)}$ (Typ)	VDSS
5A	1.8Ω	650V

Applications:

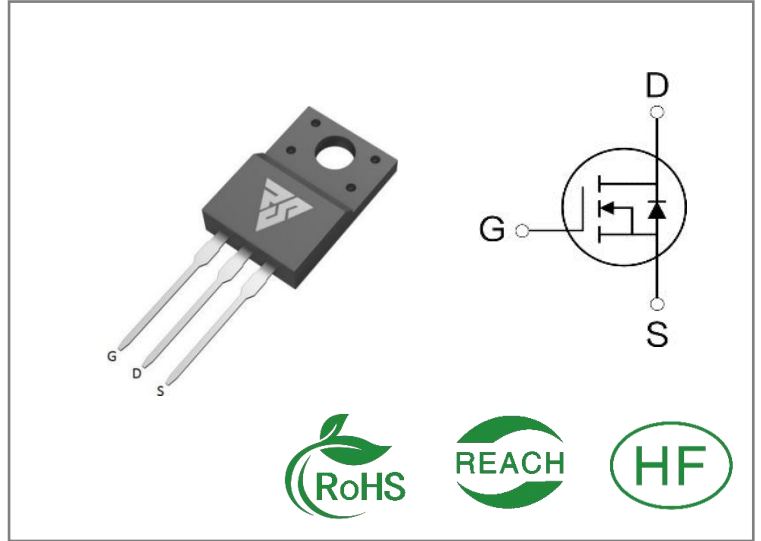
- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS5N65F	T0-220F	RS5N65F	Tube	50 PCS


Absolute Maximun Ratings $T_c = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	RS5N65F	Units
VDSS	Drain-to-Source Voltage	650	V
ID	Continuous Drain Current $T_C = 25^{\circ}\text{C}$	5	A
IDM	Pulsed Drain Current (Note*1)	20	
PD	Power Dissipation	32	W
VGS	Gate- to- Source Voltage	± 30	V
EAS	Single Pulse Avalanche Engergy $L = 10\text{mH}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$	217	mJ
TL TPKG	Maximum Temperature for Soldering	300	$^{\circ}\text{C}$
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS5N65F	Units	Test Conditions
R θ JC	Junction-to-Case	3.91	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\text{C}$
R θ JA	Junction-to- Ambient	62		1 cubic foot chamber,free air.

OFF Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650	--	--	V	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	$V_{DS}=650\text{V}, V_{GS}=0\text{V}$
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	$V_{GS}=30\text{V}, V_{DS}=0\text{V}$
	Gate- to- Source Reverse Leakage	--	--	-100		$V_{GS}=-30\text{V}, V_{DS}=0\text{V}$

ON Characteristics $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	1.8	2.1	Ω	$V_{GS}=10\text{V}, I_D=2.5\text{A}$
VGS(TH)	Gate Threshold Voltage	3	--	4	V	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	35	--	nS	$V_{DS}=325\text{V}$ $I_D=5\text{A}$ $R_G=25\Omega$
trise	Rise Time	--	8	--		
td(OFF)	Turn- OFF Delay Time	--	70	--		
tfall	Fall Time	--	22	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	595	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	60	--		
Crss	Reverse Transfer Capacitance	--	7	--		
Qg	Total Gate Charge	--	20	--	nC	VDS=520V ID=5A VGS=10V
Qgs	Gate- to- Source Charge	--	3	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	10.5	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	5	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	20	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=2.5A,VGS=0V
trr	Reverse Recovery Time	--	320	--	nS	VGS=0V IS=5A,di/dt=100A/ μs
Qrr	Reverse Recovery Charge	--	2.4	--	μC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$

Typical Feature Curve

Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

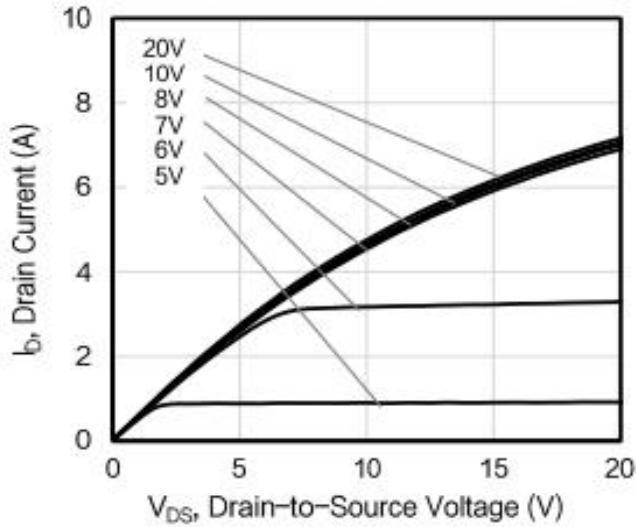


Figure 2. Body Diode Forward Voltage

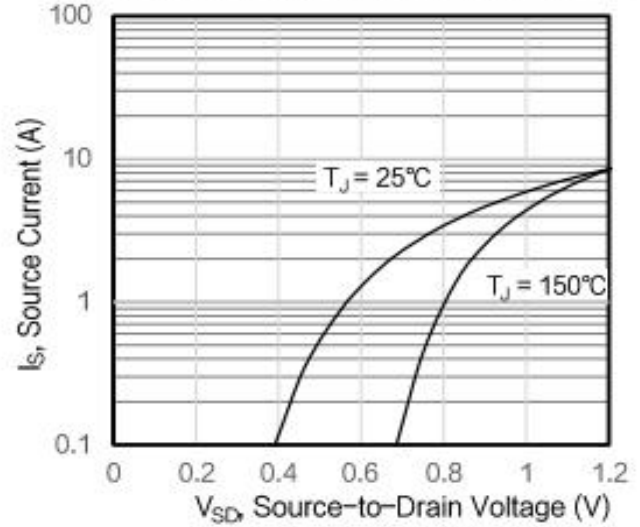


Figure 3. Drain Current vs. Temperature

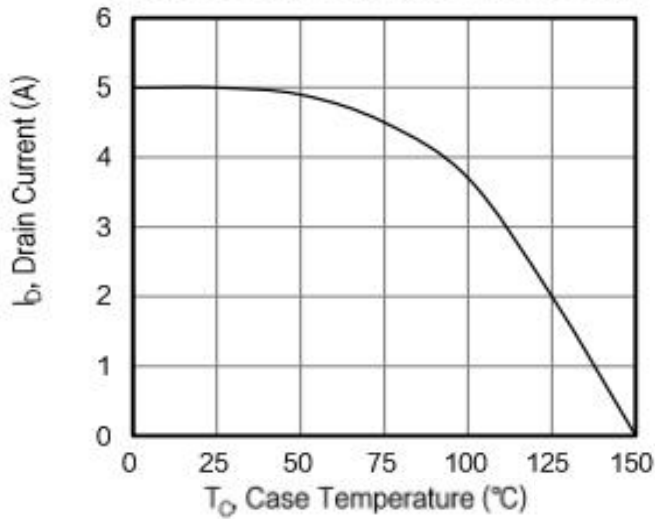


Figure 4. BV_{DSS} Variation vs. Temperature

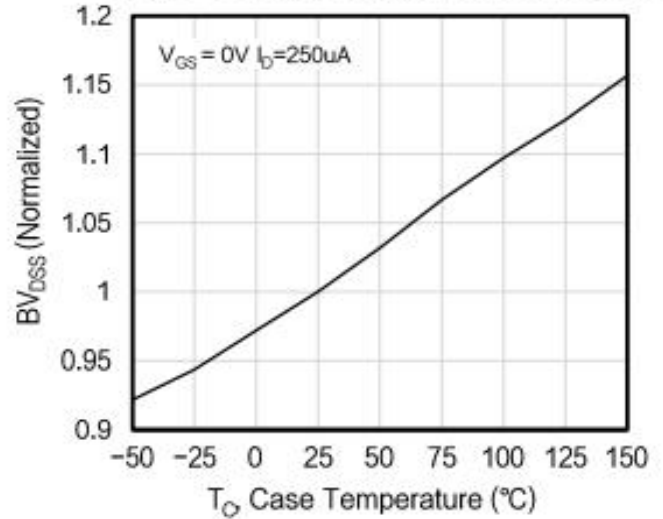


Figure 5. Transfer Characteristics

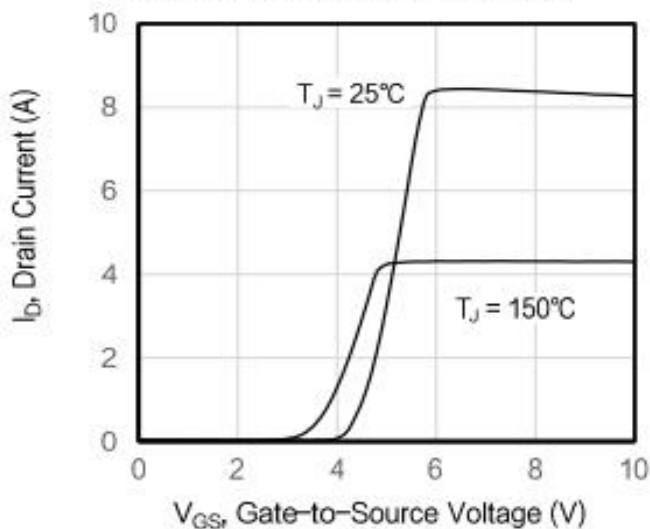


Figure 6. On-Resistance vs. Temperature

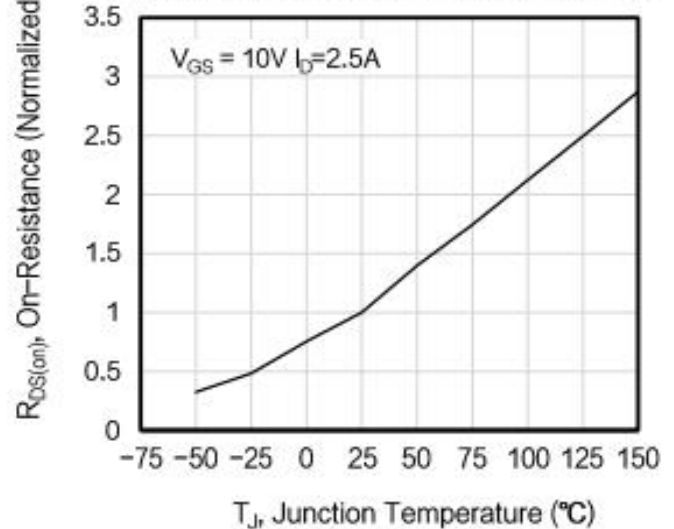


Figure 7. Capacitance

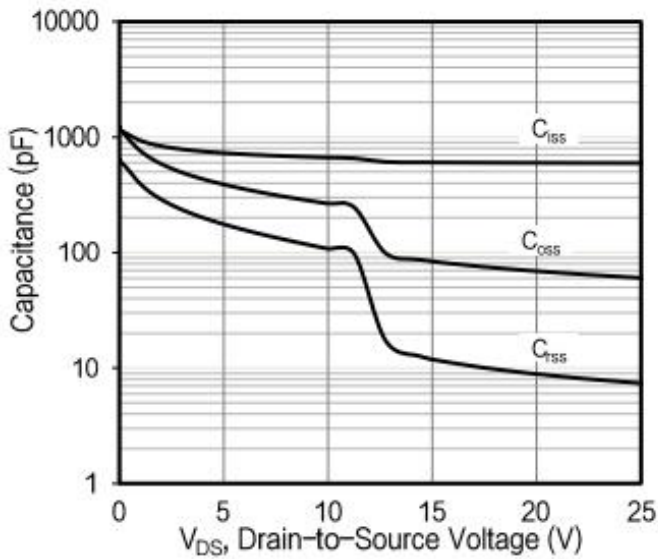


Figure 8. Gate Charge

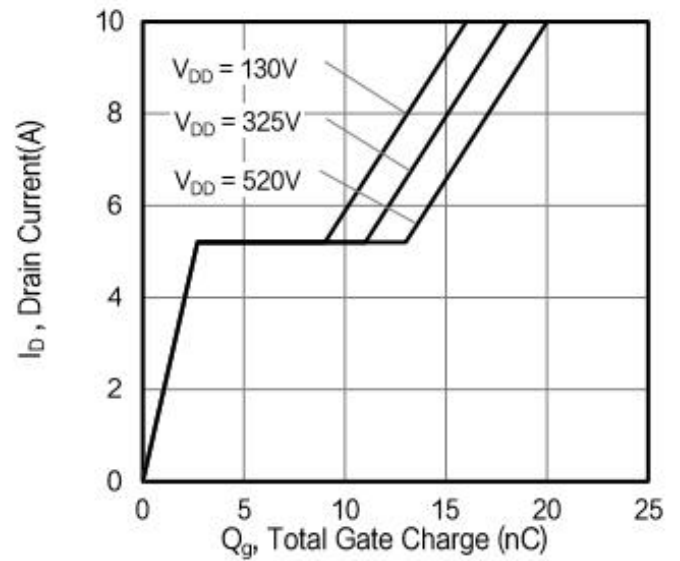


Figure 9. Transient Thermal Impedance

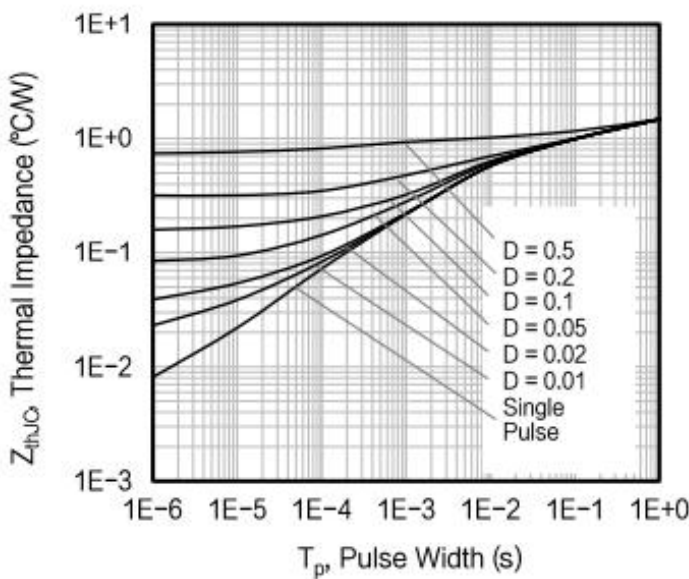
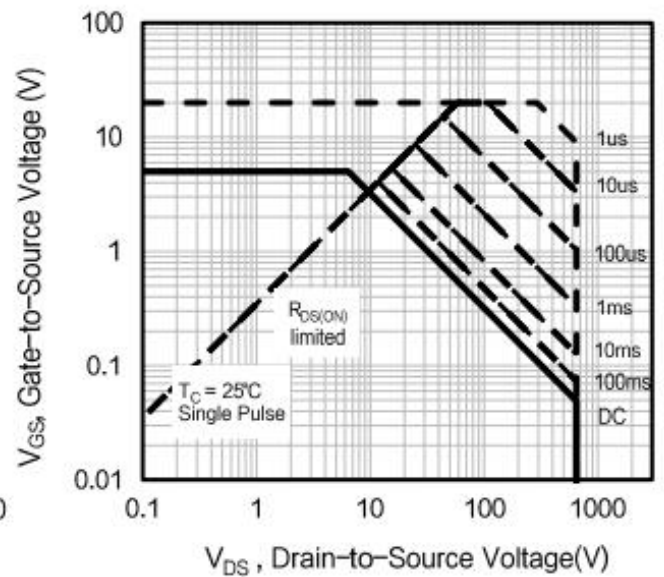


Fig. 10 Safe Operating Area



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

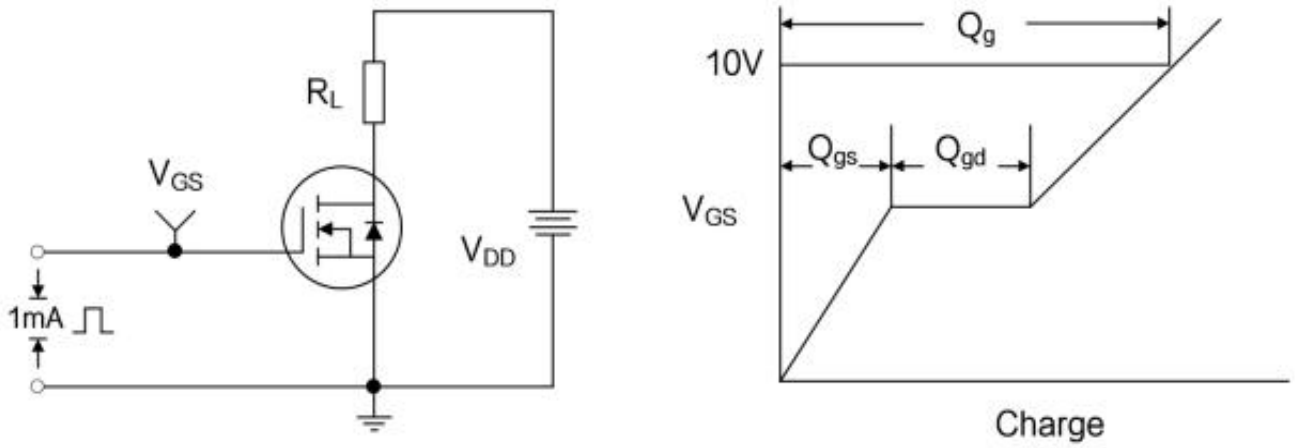


Figure B: Resistive Switching Test Circuit and Waveform

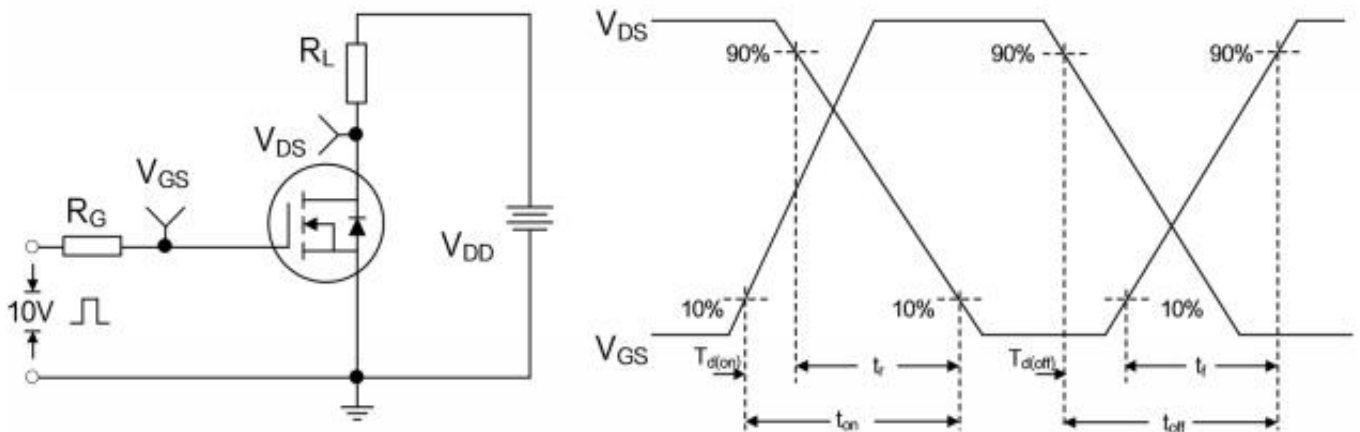
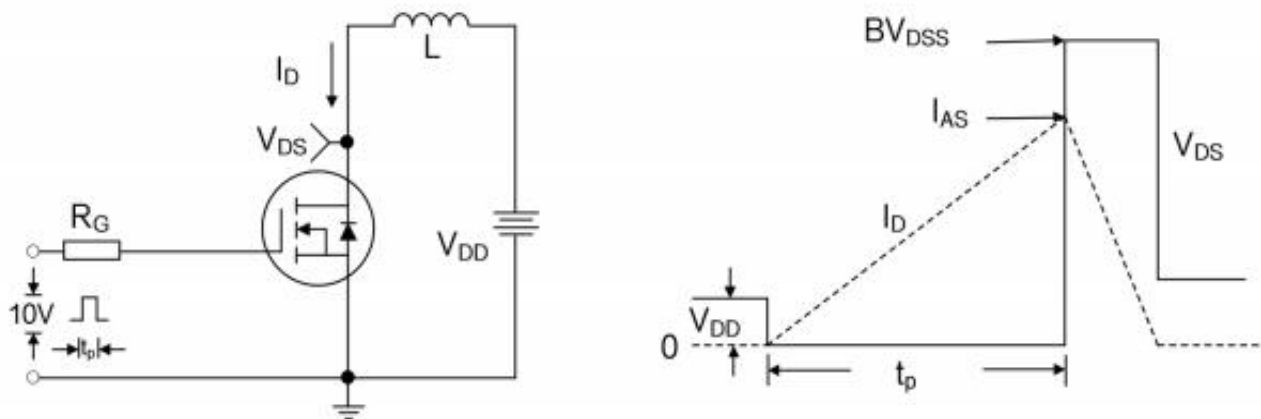
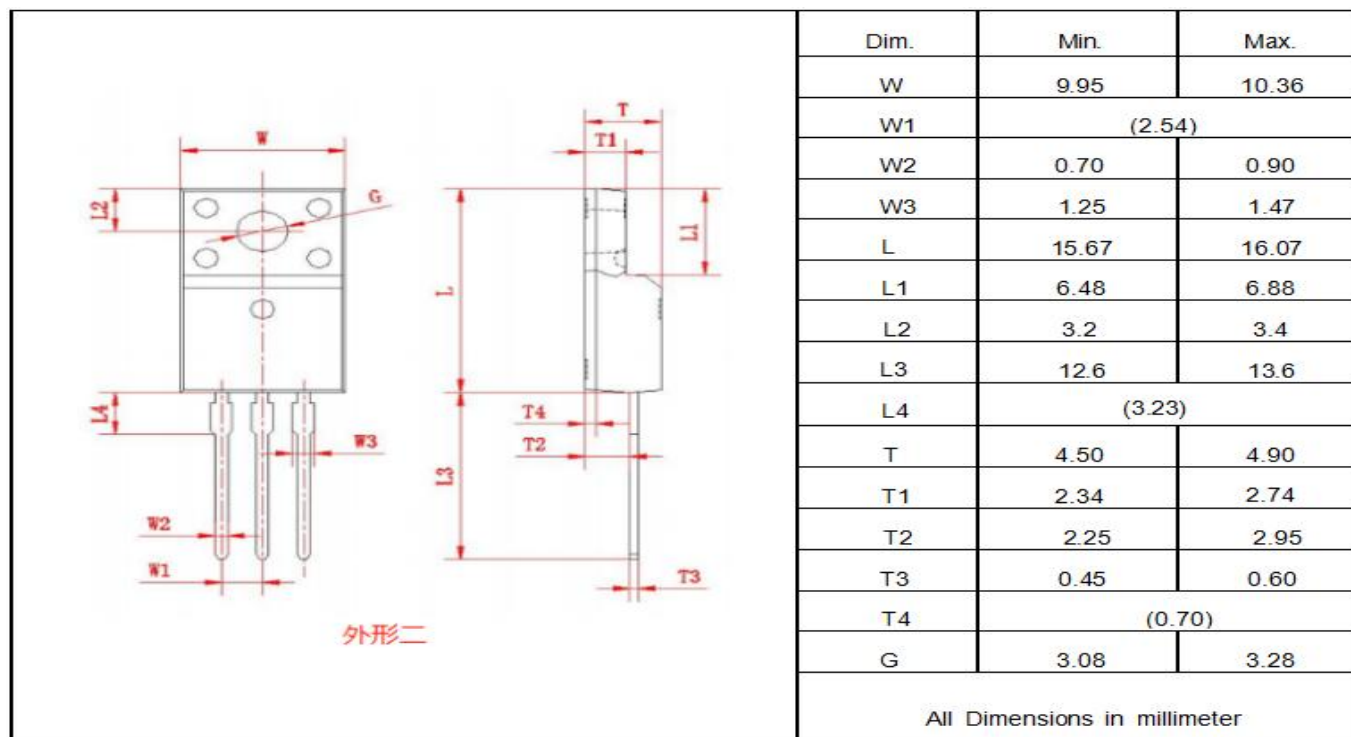
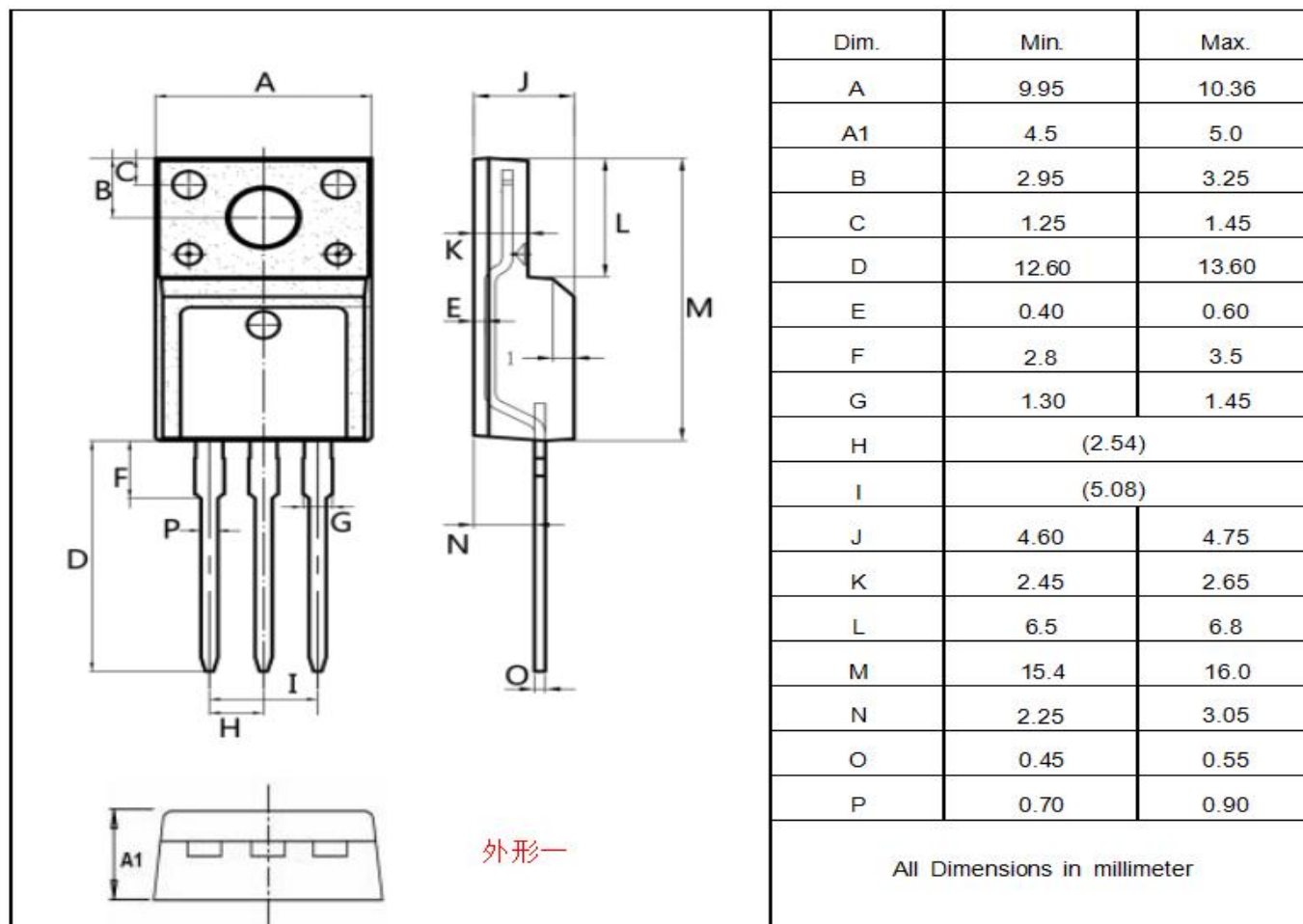


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing(TO-220F Unit: mm)



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