

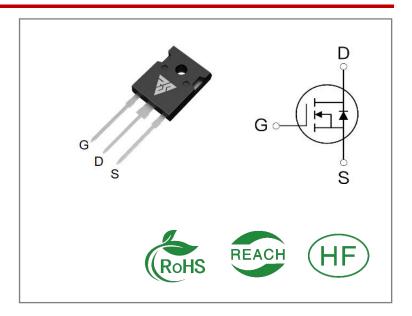
ID	R <sub>DS</sub> (ON)(Typ)	VDSS
25A	0.18Ω	500V

#### **Applications:**

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

#### **Features:**

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability



## **Ordering Information**

Part Number	Package	Marking	Packing	Qty.
RS25N50W	T0-247-3	RS25N50W	Tube	30 PCS

## Absolute Maximun Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS25N50W	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current TC=25℃	25	Δ
IDM	Pulsed Drain Current (Note*1)	100	A
PD	Power Dissipation	190	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L = 10mH,,VDD = 50V, RG = 25Ω	671	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	°C
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

<sup>\*</sup> Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.



#### **Thermal Resistance**

Symbol	Parameter	RS25N50W	Units	Test Conditions
RθJC	Junction-to-Case	0.65	°C/W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\mathrm{C}$
RθJA	Junction-to- Ambient	62.5		1 cubic foot chamber,free air.

## **OFF Characteristics** TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500			V	VGS=0V,ID=250μ A
IDSS	Drain- to- Source Leakage Current			1	μΑ	VDS=500V,VGS= 0V
IGSS	Gate- to- Source Forward Leakage			100	- A	VGS=30V ,VDS=0 V
1033	Gate- to- Source Reverse Leakage			-100	nA	VGS=-30V ,VDS= 0V

# ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On- Resistance(Note*2)		0.18	0.24	Ω	VGS=10V,ID=12. 5A
VGS(TH	Gate Threshold Voltage	3		4	V	VGS=VDS,ID=25 0μA

# Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time		53			
trise	Rise Time		37			VDS=250V
td(OFF)	Turn- OFF Delay Time		221		nS	ID=25A RG=25Ω
tfall	Fall Time		70			



**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		3134			VGS=0V
Coss	Output Capacitance		340		pF	VDS=25V
Crss	Reverse Transfer Capacitance		13			f=1.0MHz
Qg	Total Gate Charge		60.5			VDS=400V
Qgs	Gate- to- Source Charge		15.5		nC	ID=25A
Qgd	Gate-to-Drain(" Miller") Charge		22			VGS=10V

#### **Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current			25	Α	Integral pn- diode
ISM	Maximum Pulsed Current			100	Α	in MOSFET
VSD	Diode Forward Voltage			1.4	V	IS=12.5A,VGS=0V
trr	Reverse Recovery Time		375		nS	VGS=0V
Qrr	Reverse Recovery Charge		5.7		μC	IS=25A,di/dt=100 A/μs

#### Notes:

- \* 1. Repetitive rating, pulse width limited by maximum junction temperature.
- \* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%



### **Typical Feature Curve**

Figure 1. Output Characteristics (T<sub>J</sub> = 25°C)

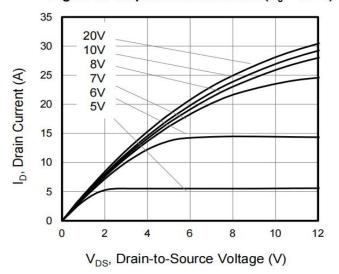


Figure 2. Body Diode Forward Voltage

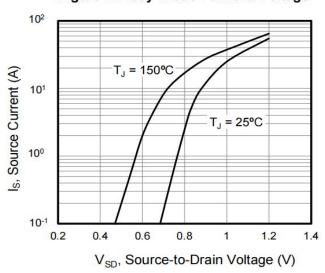


Figure 3. Drain Current vs. Temperature

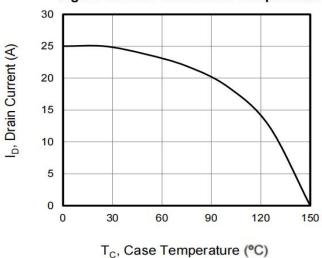


Figure 4. BV<sub>DSS</sub> Variation vs. Temperature

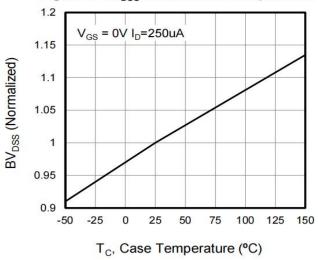


Figure 5. Transfer Characteristics

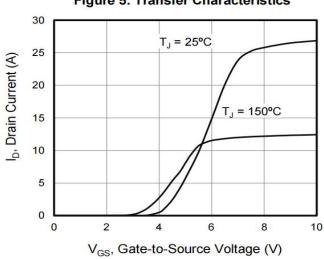
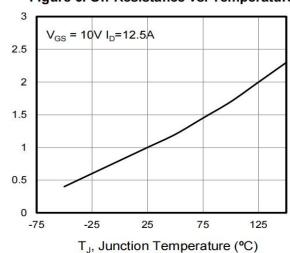
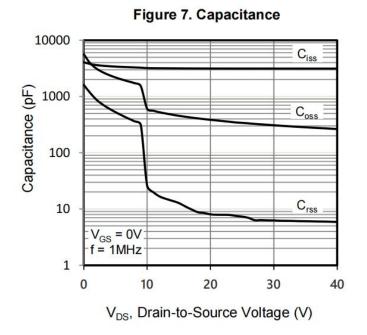


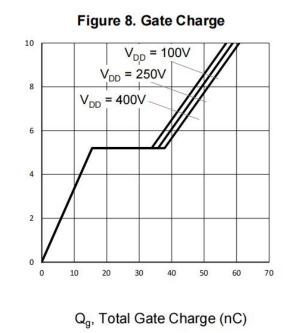
Figure 6. On-Resistance vs. Temperature



R<sub>DS(on)</sub>, On-Resistance (Normalized)

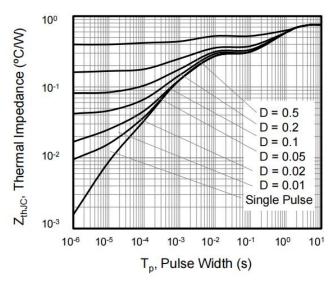








V<sub>GS</sub>, Gate-to-Source Voltage (V)





## **Test Circuits and Waveforms**

Figure A: Gate Charge Test Circuit and Waveform

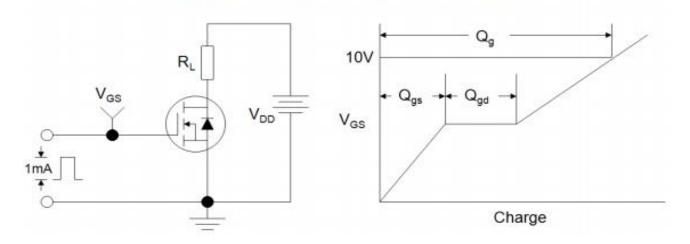


Figure B: Resistive Switching Test Circuit and Waveform

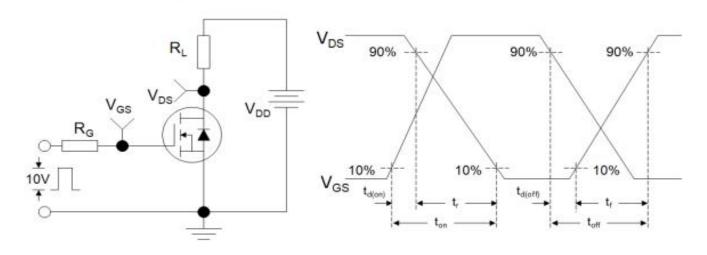
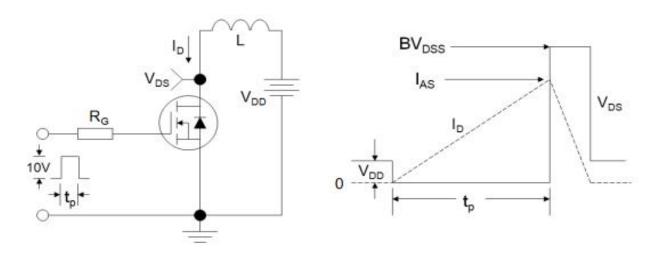
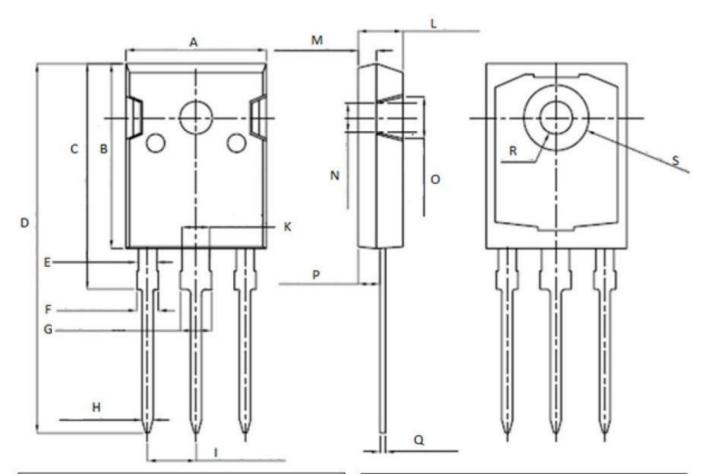


Figure C: Unclamped Inductive Switching Test Circuit and Waveform





# Package outline drawing(TO-247 Unit: mm)



	Unit: mm	
Symbol	Min.	Max.
Α	15. 95	16. 25
В	20.85	21. 25
C	20.95	21.35
D	40.5	40.9
E	1.9	2. 1
F	2. 1	2. 25
G	3. 1	3. 25
Н	1.1	1.3
ı	5. 40	5. 50

	Unit: mm					
Symbol	Min.	Max.				
K	2.90	3. 10				
L	4. 90	5. 30				
M	1.90	2. 10				
N	4.50	4. 70				
0	5. 40	5. 60				
P	2. 29	2.49				
Q	0. 51	0. 71				
R	ф3.5	ф3.7				
S	ф7.1	ф7.3				



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