

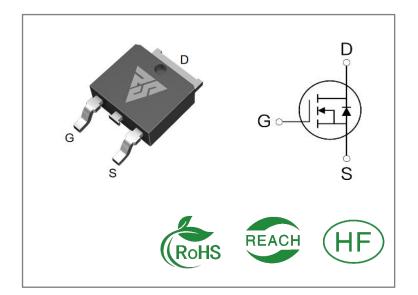
ID	R _{DS} (ON)(Typ)	VDSS
180A	$2.0 m\Omega$	30V

Applications:

- Load Switch
- PWM Applications
- Power Managment

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability



Ordering Information

Part Number	Package	Marking	Packing	Qty.	
RS30N180D	T0-252	RS30N180D	Tape&reel	2500 PCS	

Absolute Maximun Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS30N180D	Units
VDSS	Drain-to-Source Voltage	30	V
ID	Continuous Drain Current TC=25℃	180	
ID	Continuous Drain Current TC=100℃	114	Α
IDM	Pulsed Drain Current	720	
PD	Power Dissipation	80	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH,VDD = 15V, RG = 25Ω , Tj = 25° C	305	mJ
	Maximum Temperature for Soldering	300	
TL TPKG	L TPKG Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		${\mathbb C}$
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

^{*} Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.



Thermal Resistance

Symbol	Parameter	RS30N180D	Units	Test Conditions
RθJC	Junction-to-Case	2.1	°C/W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\mathrm{C}$
RθJA	Junction-to- Ambient	35		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	30			V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current			1	μΑ	VDS=30V VGS=0V
IGSS	Sate- to- Source Forward 100		^	VGS=20V VDS=0V		
	Gate- to- Source Reverse Leakage				nA	VGS=-20V VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter		Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On- Resistance		2.0	2.5	mΩ	VGS=10V,ID=30A
			3.3	4.3	mΩ	VGS=4.5V ID=20A
VGS(TH)	Gate Threshold Voltage	1.3	1.9	2.5	V	VGS=VDS ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time		16			\/D0_45\/
trise	Rise Time		30			VDS=15V ID=30A
td(OFF)	Turn- OFF Delay Time		52		nS	RG=3Ω VGS=10V
tfall	Fall Time		20			vG2=10V



Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions	
Ciss	Input Capacitance		5060			VGS= 0V	
Coss	Output Capacitance		570		рF	VDS=15V	
Crss	Reverse Transfer Capacitance		470			f=1.0MHz	
Qg	Total Gate Charge		75			VDS= 15V	
Qgs	Gate- to- Source Charge		9		nC	ID=20A	
Qgd	Gate-to-Drain(" Miller") Charge		18			VGS=10V	

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current		-	180	Α	Integral pn- diode
ISM	Maximum Pulsed Current			720	Α	in MOSFET
VSD	Diode Forward Voltage			1.2	V	IS=30A,VGS=0V
trr	Reverse Recovery Time		24		nS	VGS=0V
Qrr	Reverse Recovery Charge		14		nC	IS=30A di/dt=100A/μs

Notes:

^{* 1.} Repetitive rating, pulse width limited by maximum junction temperature.

^{* 2.} Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%



Typical Feature Curve

Figure 1: Output Characteristics

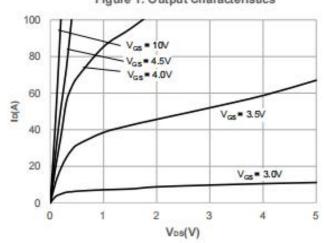


Figure 2: Typical Transfer Characteristics

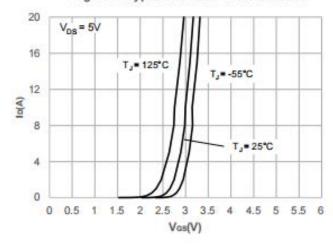


Figure 3: On-resistance vs. Drain Current

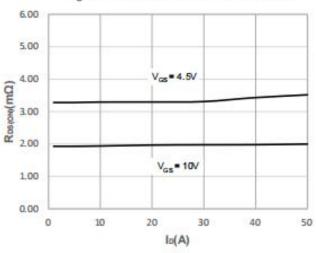


Figure 4: Body Diode Characteristics

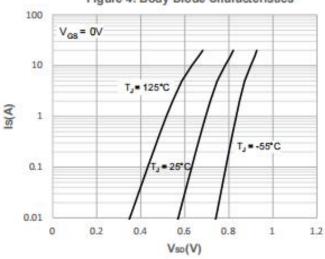


Figure 5: Gate Charge Characteristics

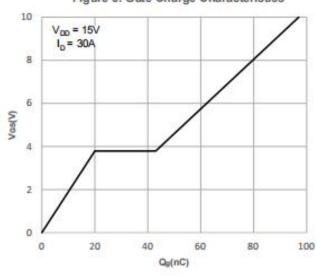
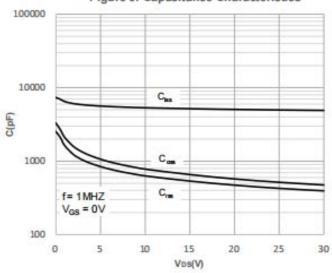


Figure 6: Capacitance Characteristics



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Figure 7: Normalized Breakdown voltage vs. Junction Temperature

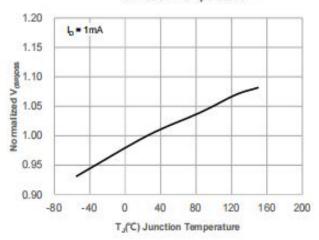


Figure 8: Normalized on Resistance vs. Junction Temperature

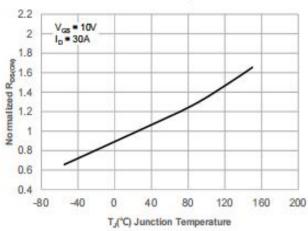


Figure 9: Maximum Safe Operating Area

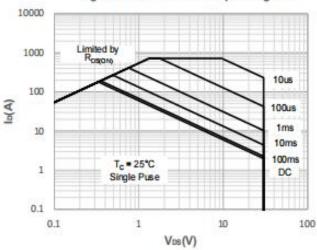


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

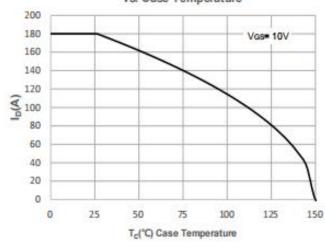


Figure 11: Normalized Maximum Transient Thermal Impedance

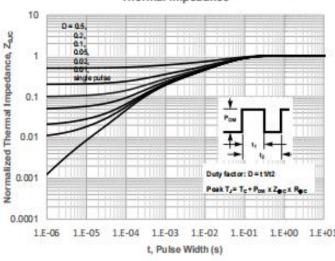
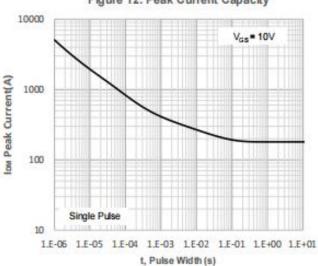


Figure 12: Peak Current Capacity



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Test ircuits and Waveforms

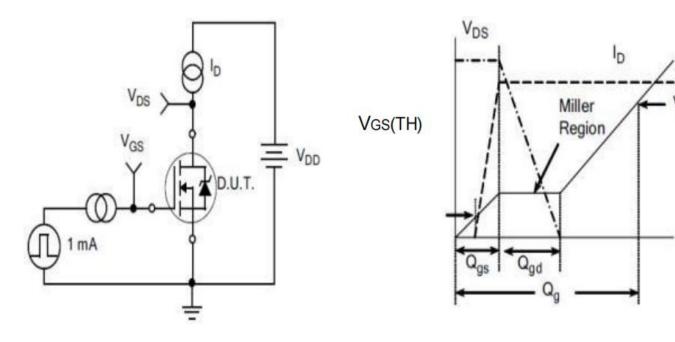


Figure A. Gate Charge Test Circuit

VDS - V_{GS} E VDD RG D.U.T.

Figure C. Resistive Switching Test Circuit

10% VGS t_{d(OFF)} t_{fall} td(ON) trise

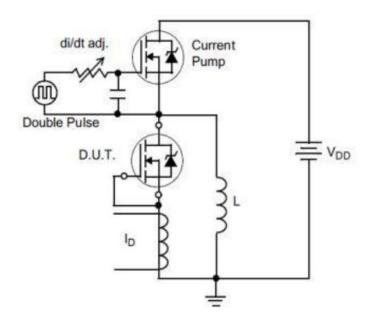
Figure B.

Gate Charge Waveform

Figure D. Resistive Switching Waveforms



Test ircuits and Waveforms



 $di/dt = 100A/\mu A$ Q_{rr}

Figure E.Diode Reverse Recovery Test Circuit

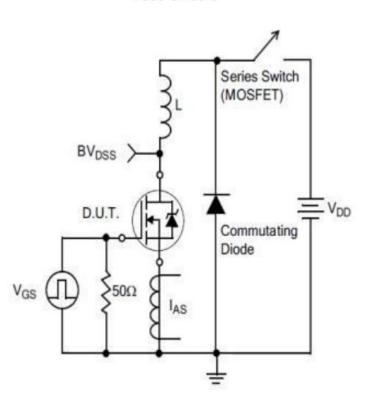


Figure F.Diode Reverse Recovery Waveform

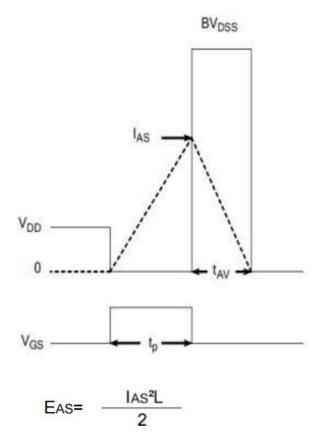
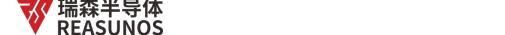
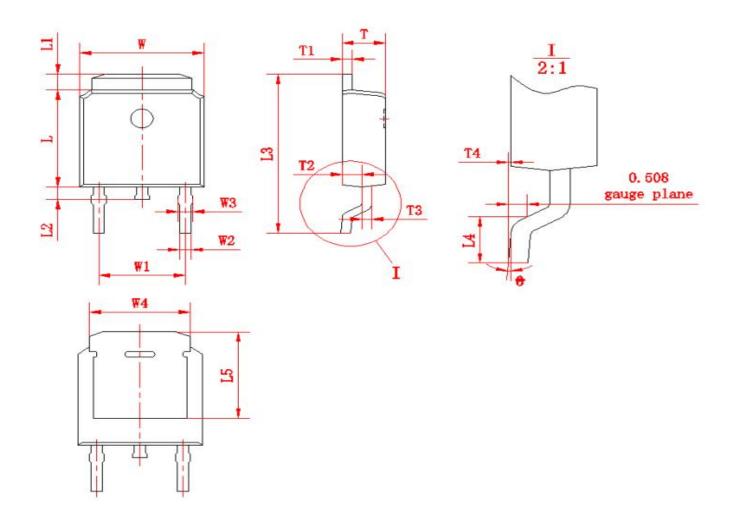


Figure G.Unclamped Inductive Switching Test Circuit

Figure H.Unclamped Inductive Switching Waveforms



Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
<u> </u>	Min	Max	17 15	Min	Max	1) 2	Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.5	572)	L2	2 0.60 1.00		T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	Т3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5	.3)	L5	(5.20)		0	0	8
L	6.00	6.20	Т	2.20	2.40			



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