

ID	R _{DS} (ON)(Typ)	VDSS
50A	12mΩ	60V

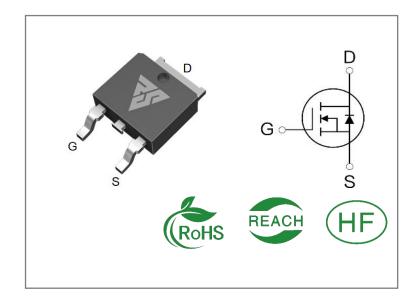
Applications:

- Load Switch
- PWM Applications
- Power Managment

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability





Part Number	Package	Marking	Packing	Qty.
RS60N50D	T0-252	RS60N50D	Tape&reel	2500 PCS

Absolute Maximun Ratings Tc= 25℃ unless otherwise specified

Symbol	Parameter	RS60N50D	Units
VDSS	Drain-to-Source Voltage	60	V
ID	Continuous Drain Current TC=25℃	50	
ID	Continuous Drain Current TC=100℃	33	Α
IDM	Pulsed Drain Current (Note*1)	200	
PD	Power Dissipation	75	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy	81	mJ
	Maximum Temperature for Soldering	300	
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds	260	200
	Package Body for 10 seconds		$^{\circ}\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!$
TJ and	Operating Junction and Storage	-55 to 175	
TSTG	Temperature Range	-33 (01/3	

^{*} Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.



Thermal Resistance

Symbol	Parameter	RS60N50D	Units	Test Conditions
				Drain lead soldered to water cooled
ROJC	Junction-to-Case	2	°C/W	heatsink, PD adjusted for a peak
				junction temperature of + 1 5 0 $^\circ \! \mathbb{C}$

OFF Characteristics TJ= 25[°]C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage				V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current			1	μΑ	VDS=60V,VGS=0V
	Gate- to- Source Forward Leakage			100		VGS=20V ,VDS=0V
IGSS	Gate- to- Source Reverse Leakage			-100	nA	VGS=-20V VDS=0V

ON Characteristics TJ=25 °C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
DDS(on)	Static Drain- to- Source On-	1	12	17	mΩ	VGS=10V,ID=30A
RDS(on) Resistance(Note*2)	Resistance(Note*2)		16	25	mΩ	VGS=4.5V,ID=20A
VGS(TH)	Cata Thurshald Valtage	1.0	1 /	2.5	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	VGS=VDS
	Gate Threshold Voltage	1.0	1.6	2.5	V	ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time		11			
trise	Rise Time		79			VDS=30V
td(OFF)	Turn- OFF Delay Time		33		nS	ID=30A RG=1.8Ω
tfall	Fall Time		107			



Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		2030	1		VGS=0V
Coss	Output Capacitance		130	1	pF	VDS=25V
Crss	Reverse Transfer Capacitance		115			f=1.0MHz
Qg	Total Gate Charge		45			VDS=30V
Qgs	Gate- to- Source Charge		8		nC	ID=30A
Qgd	Gate-to-Drain(" Miller") Charge		11			VGS=10V

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current			50	Α	Integral pn- diode
ISM	Maximum Pulsed Current			200	Α	in MOSFET
VSD	Diode Forward Voltage			1.2	V	IS=30A,VGS=0V
trr	Reverse Recovery Time		14		nS	VGS=0V
Qrr	Reverse Recovery Charge		10		nC	IS=30A di/dt=100A/μs

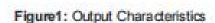
Notes:

^{* 1.} Repetitive rating, pulse width limited by maximum junction temperature.

^{* 2.} Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 0.5%



Typical Feature Curve



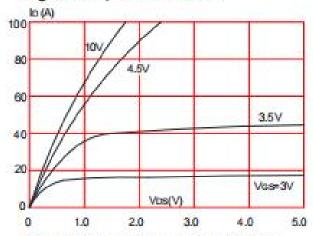


Figure 3: On-resistance vs. Drain Current

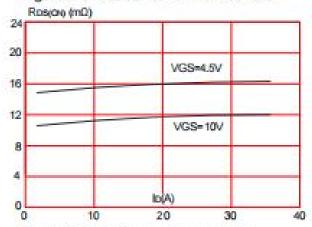


Figure 5: Gate Charge Characteristics

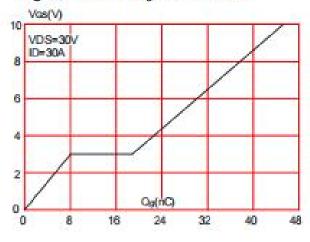


Figure 2: Typical Transfer Characteristics

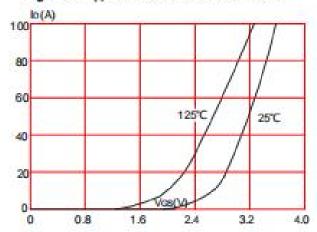


Figure 4: Body Diode Characteristics

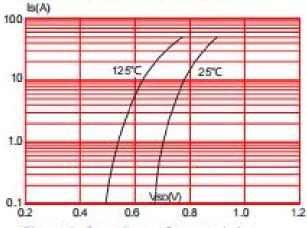


Figure 6: Capacitance Characteristics

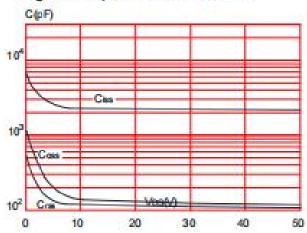




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

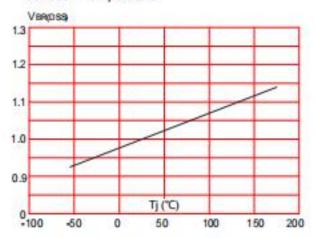


Figure 9: Maximum Safe Operating Area

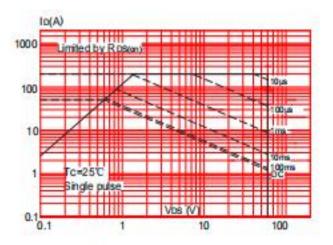


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

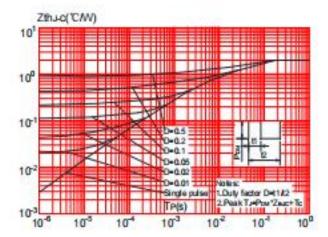


Figure 8: Normalized on Resistance vs. Junction Temperature

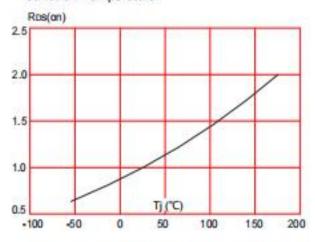
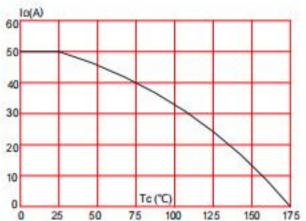


Figure 10: Maximum Continuous Drain Current vs. Case Temperature





Test ircuits and Waveforms

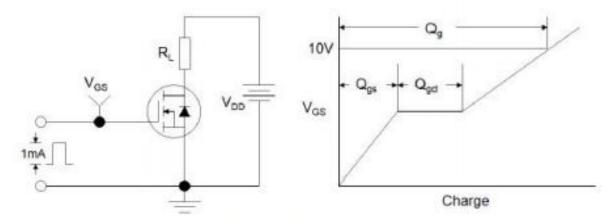


Figure1:Gate Charge Test Circuit & Waveform

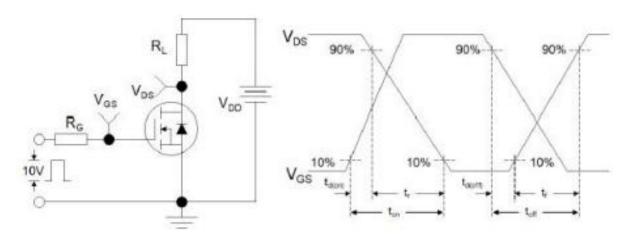


Figure 2: Resistive Switching Test Circuit & Waveforms

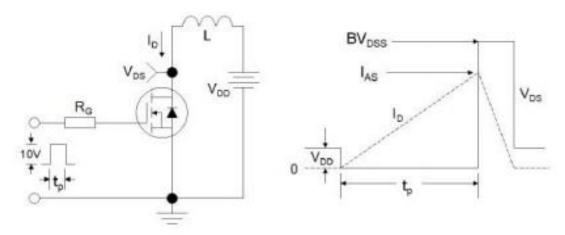
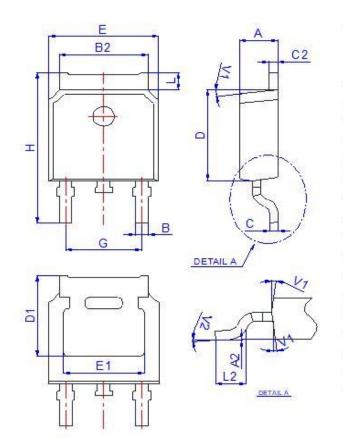


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package outline drawing(TO-252 Unit: mm)



	Dimensions							
Ref.	11	Millimete	ers		Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.		
Α	2.10		2.50	0.083		0.098		
A2	0	2	0.10	0		0.004		
В	0.66		0.86	0.026		0.034		
B2	5.18		5.48	0.202		0.216		
С	0.40	3	0.60	0.016		0.024		
C2	0.44		0.58	0.017		0.023		
D	5.90		6.30	0.232		0.248		
D1		5.30REF			.209RE	F		
E	6.40		6.80	0.252		0.268		
E1	4.63			0.182				
G	4.47		4.67	0.176		0.184		
Н	9.50	2	10.70	0.374		0.421		
L	1.09		1.21	0.043		0.048		
L2	1.35		1.65	0.053		0.065		
V1	18	7°		3	7°			
V2	0°		6°	0°		6°		



Disclaimers:

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information in current and complete. All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale. Testing, reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement, testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using Reasunos's components. To minimize risk, customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights, nor the rights of others. Reproduction of inform- ation in Reasunos's data sheets or data books is permissible only if reproduction is without modification oralteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.

As used herein:

- 1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.
- 2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.