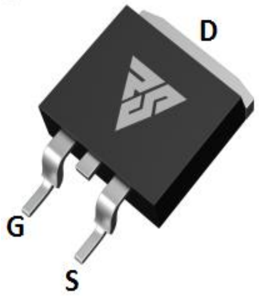
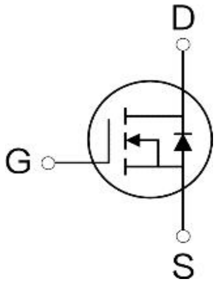
ID	R_{DS}(ON)(Typ)	VDSS
135A	4.2mΩ	100V

Applications:
- Load Switch
- PWM Applications
- Power Managment

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability





Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS100N135HS	T0-263	RS100N135HS	Tape&reel	800 PCS

Absolute Maximun Ratings **Tc= 25℃ unless otherwise specified**

Symbol	Parameter	RS100N135HS	Units
VDSS	Drain-to-Source Voltage	100	V
ID	Continuous Drain Current TC=25℃	135	A
ID	Continuous Drain Current TC=100℃	91	
IDM	Pulsed Drain Current	540	
PD	Power Dissipation	167	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH,VDS = 50V, RG = 25Ω, Tj = 25℃	136	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS100N135HS	Units	Test Conditions
RθJC	Junction-to-Case	0.75	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	62		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	100	--	--	V	VGS=0V,ID=250µA
IDSS	Drain- to- Source Leakage Current	--	--	1	µA	VDS=80V,VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	4.2	5	mΩ	VGS=10V,ID=20A
		--	6	8	mΩ	VGS=4.5V,ID=10A
VGS(TH)	Gate Threshold Voltage	2.0	--	4.0	V	VGS=VDS,ID=250µA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	28	--	nS	VDS=50V ID=50A RG=3Ω VGS=10V
trise	Rise Time	--	24	--		
td(OFF)	Turn- OFF Delay Time	--	64	--		
tfall	Fall Time	--	22	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	3610	--	pF	VGS= 0V VDS=50V f=1MHz
Coss	Output Capacitance	--	1240	--		
Crss	Reverse Transfer Capacitance	--	32	--		
Qg	Total Gate Charge	--	65.5	--	nC	VDS= 50V ID=50A VGS=10V
Qgs	Gate- to- Source Charge	--	16	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	20	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	135	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	540	A	
VSD	Diode Forward Voltage	--	--	1.0	V	IS=20A,VGS=0V
trr	Reverse Recovery Time	--	95	--	nS	VGS=0V IS=20A di/dt=100A/µs
Qrr	Reverse Recovery Charge	--	63	--	nC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.

* 2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 1.5%

Typical Feature Curve

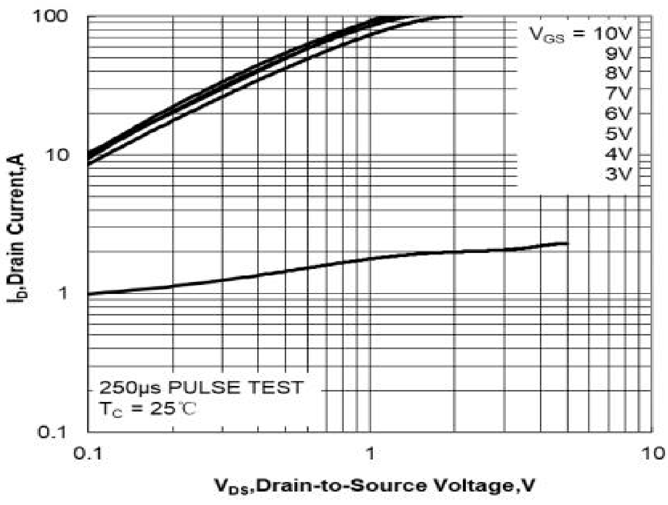


Figure 1. Output Characteristics

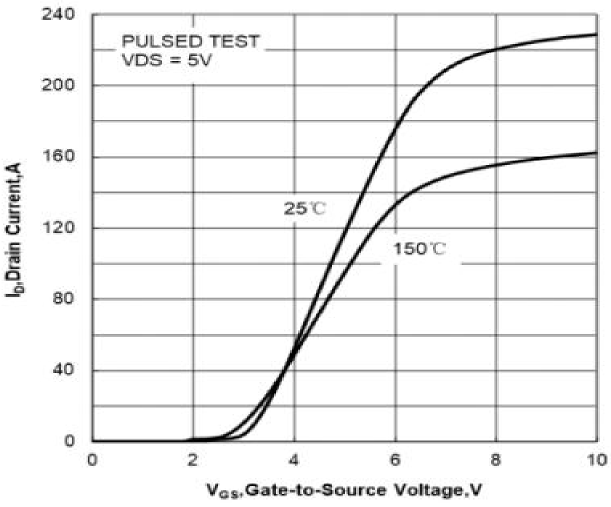


Figure 2. Transfer Characteristics

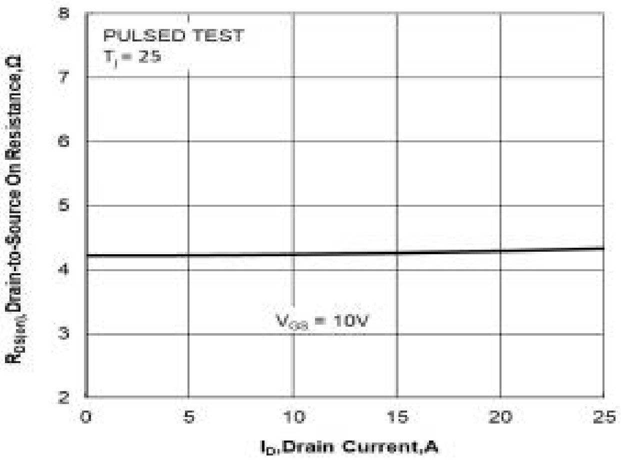


Figure 3. Drain-to-Source On Resistance
vs Drain Current

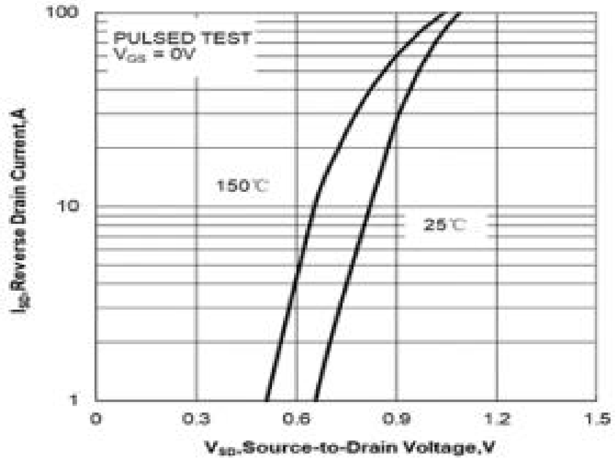


Figure 4. Body Diode Forward Voltage
vs Source Current and Temperature

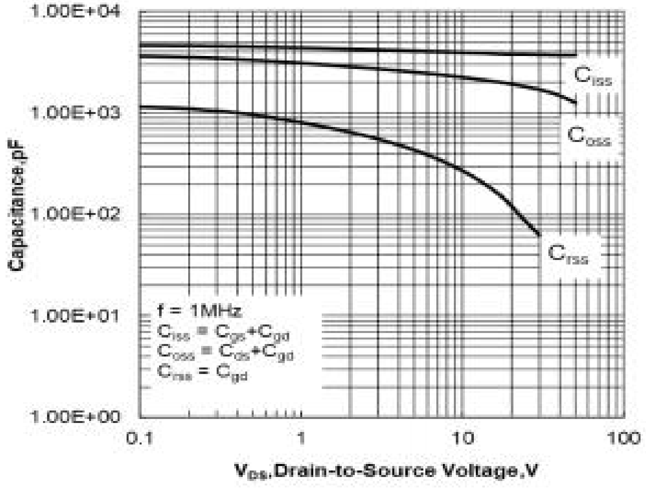


Figure 5. Capacitance Characteristics

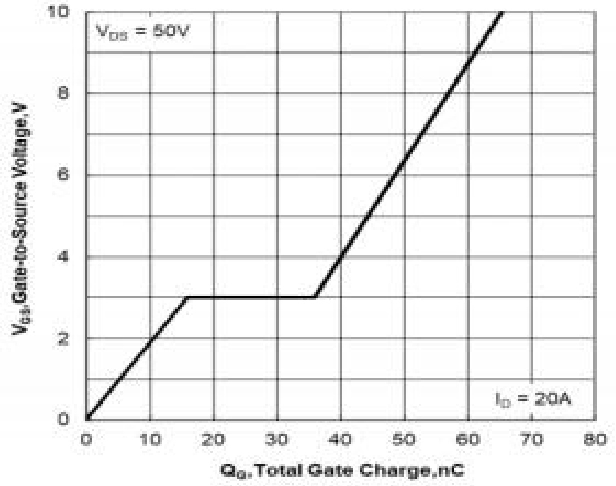


Figure 6. Gate Charge Characteristics

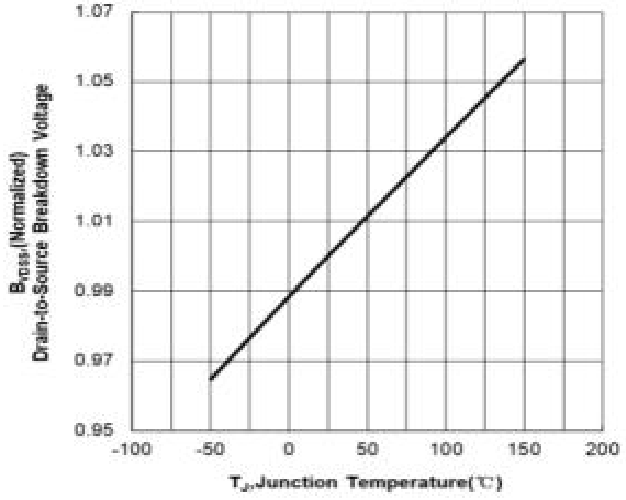


Figure 7. Normalized Breakdown Voltage
vs Junction Temperature

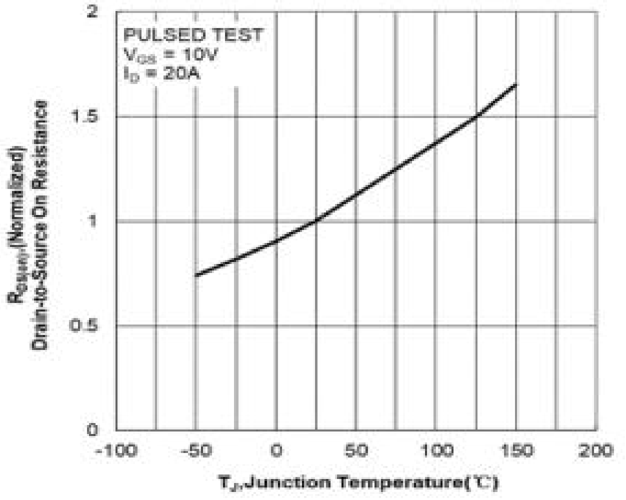


Figure 8. Normalized On Resistancevs
Junction Temperature

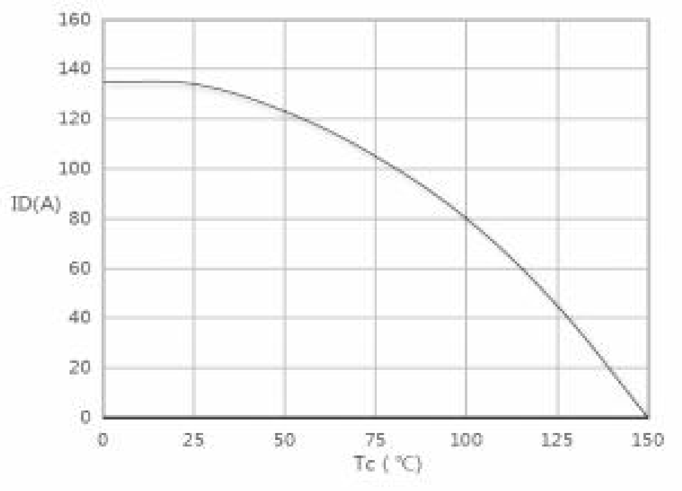


Figure 9. Maximum Continuous Drain Current vs Case Temperature

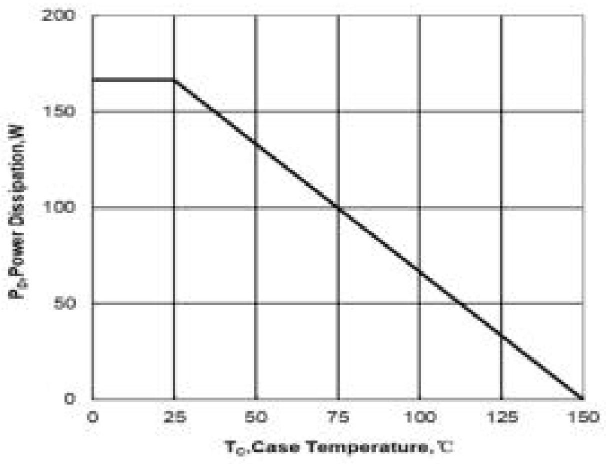


Figure 10. Maximum Power Dissipation vs Case Temperature

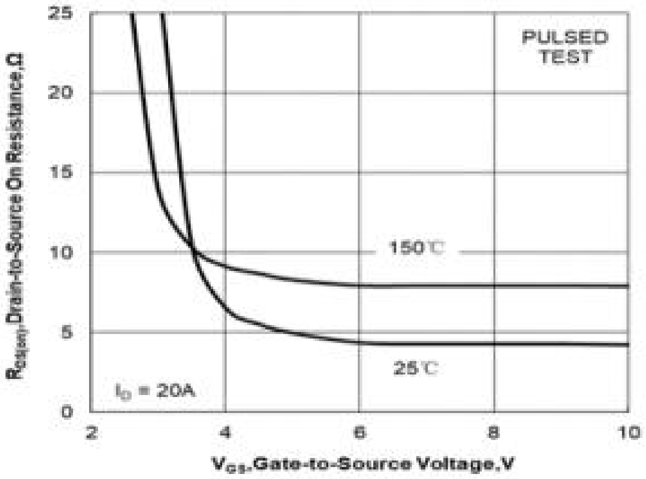


Figure11. Drain-to-Source On Resistancevs Gate Voltage and Drain Current

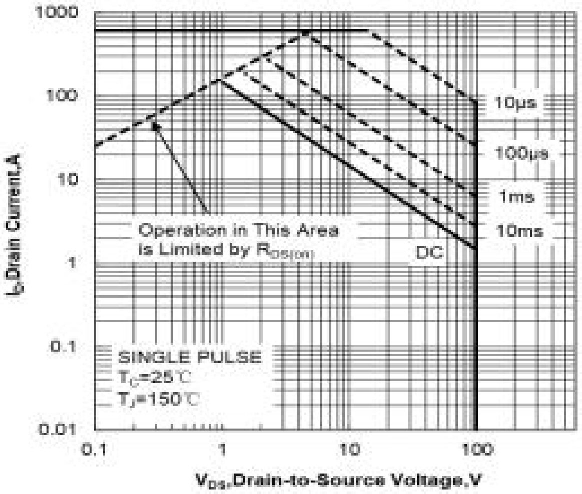


Figure 12. Maximum Safe Operating Area

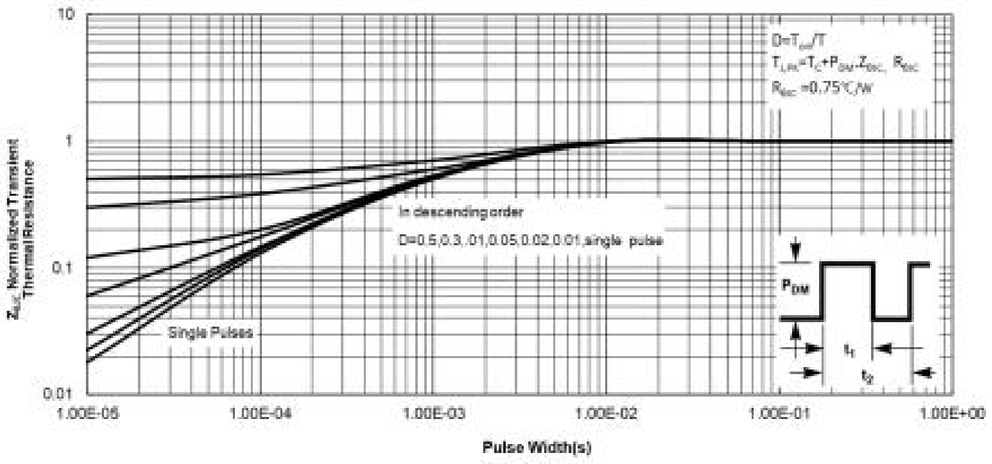


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test ircuits and Waveforms

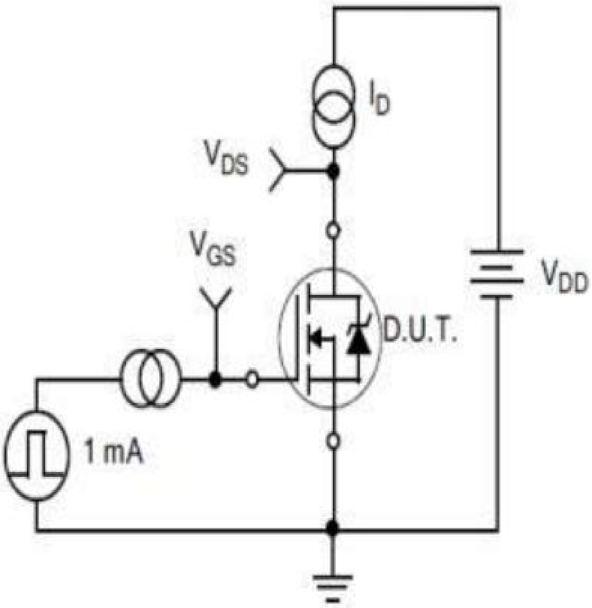


Figure A.
Gate Charge Test Circuit

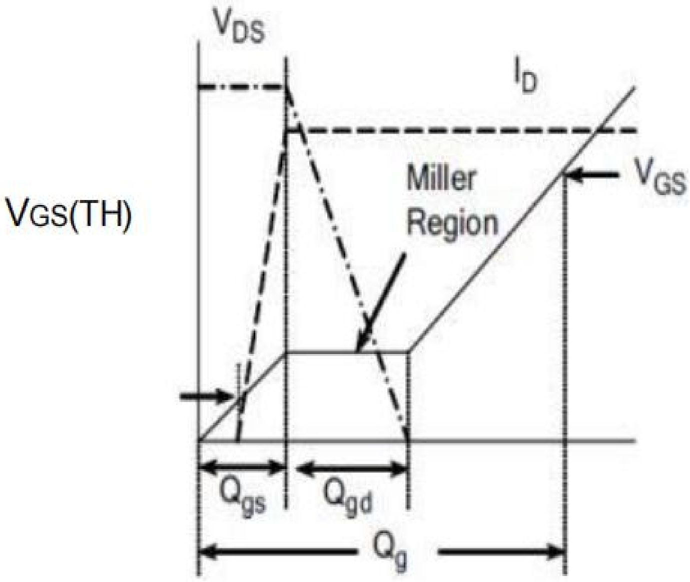


Figure B.
Gate Charge Waveform

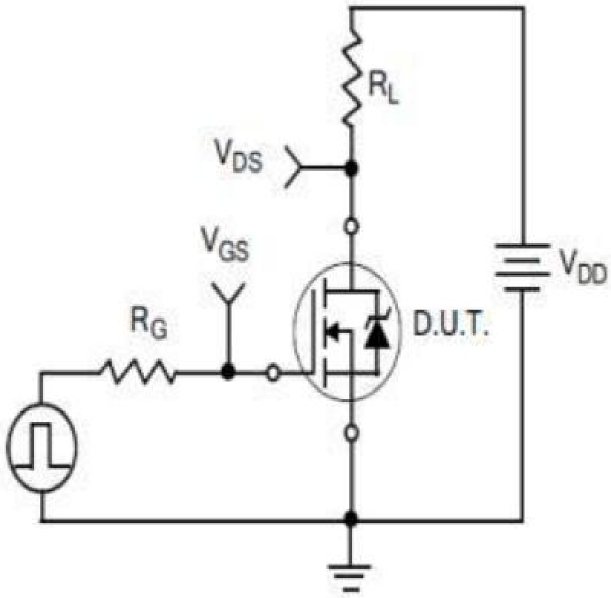


Figure C.
Resistive Switching Test Circuit

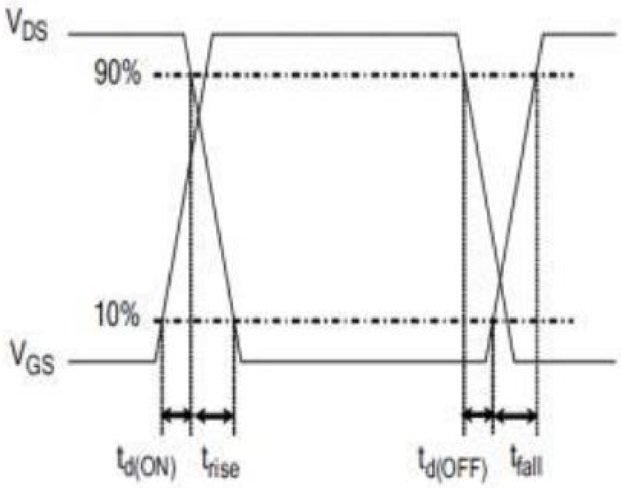


Figure D.
Resistive Switching Waveforms

Test ircuits and Waveforms

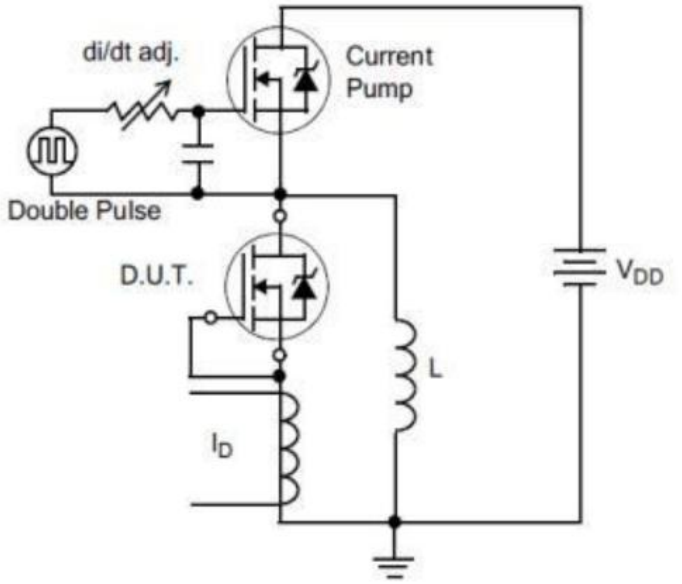


Figure E.Diode Reverse Recovery Test Circuit

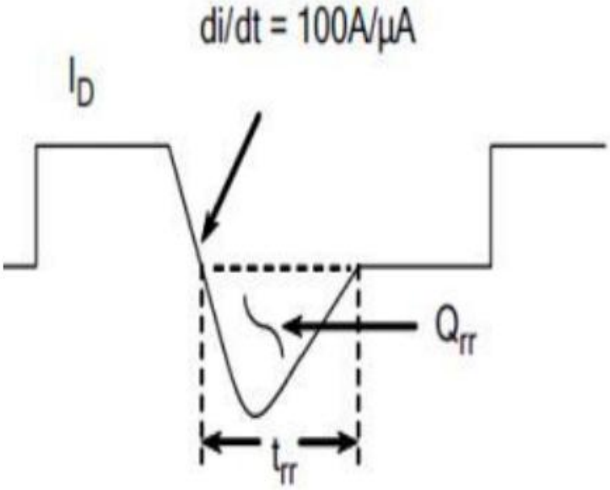
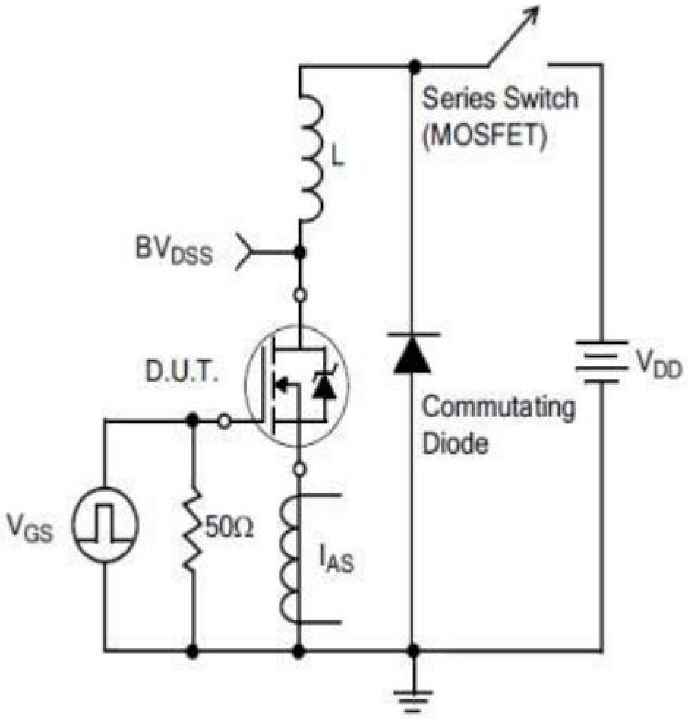
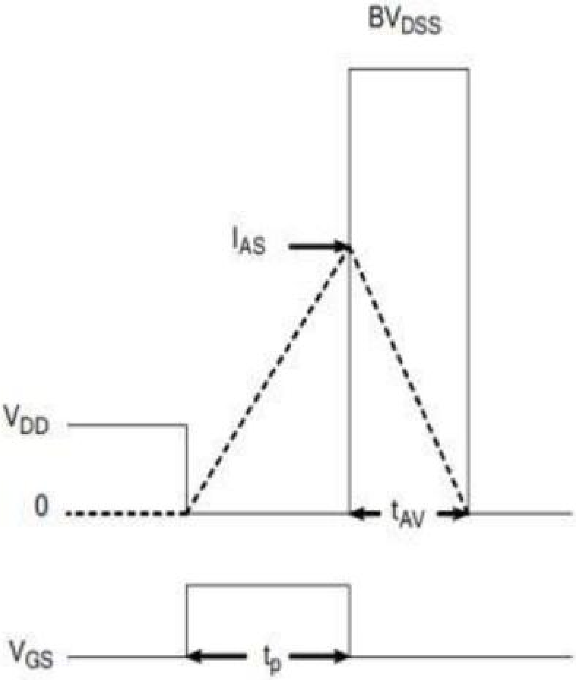


Figure F.Diode Reverse Recovery Waveform



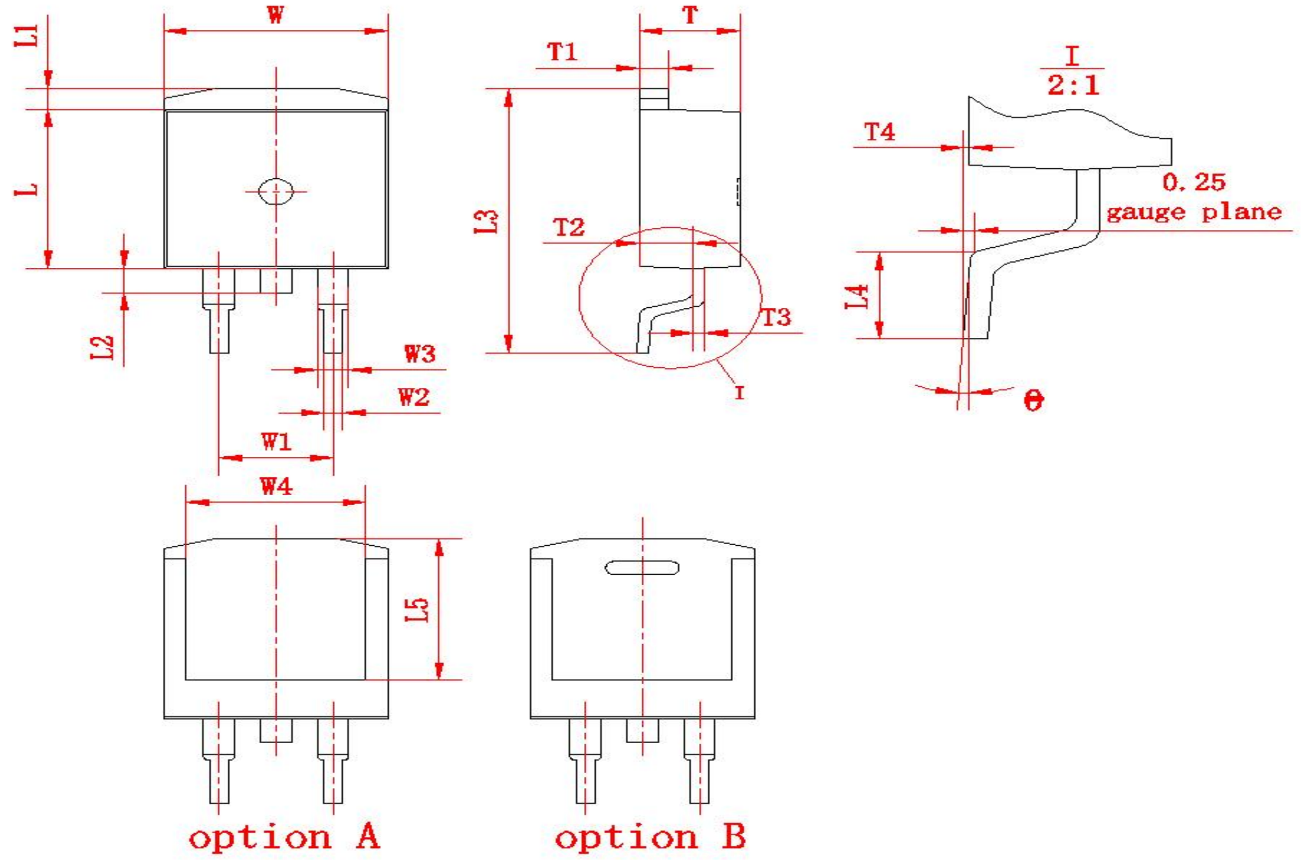


$$E_{AS}=\frac{I_{AS}^2L}{2}$$

Figure G.Unclamped Inductive Switching Test Circuit

Figure H.Unclamped Inductive Switching Waveforms

Package outline drawing(TO-263 Unit: mm)



(单位: mm)

符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	9.80	10.20	L1	1.00	1.40	T1	1.20	1.40
W1	(5.08)		L2	1.20	1.60	T2	2.20	2.60
W2	0.70	0.95	L3	15.00	15.60	T3	0.45	0.65
W3	1.17	1.62	L4	2.20	2.80	T4	0	0.25
W4	(8.0)		L5	(8.2)		θ	0°	8°
L	9.00	9.40	T	4.30	4.70			

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