

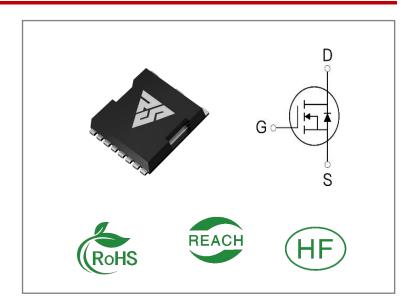
ID	R <sub>DS</sub> (ON)(Typ)	VDSS
210A	$1.9$ m $\Omega$	105V

## **Applications:**

- Load Switch
- PWM Applications
- Power Managment

#### **Features:**

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability



**Ordering Information** 

Part Number	Package	Marking	Packing	Qty.
RS105N210I	TOLL-8L	RS105N210I	Tape&reel	2000 PCS

## Absolute Maximun Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS105N210I	Units
VDSS	Drain-to-Source Voltage	105	V
ID	Continuous Drain Current TC=25°C Notes *1)	210	
ID	Continuous Drain Current TC=100℃	121	Α
IDM	Pulsed Drain Current Notes *2)	772	
PD	Power Dissipation	178	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy Notes *3) L = 0.5mH,VDD =50V, RG = $25\Omega$ , Tj = $25^{\circ}$ C	1536	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	$^{\circ}$
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

<sup>\*</sup> Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the Absolute Maximum Ratings" Table may cause permanent damage to the device.



## **Thermal Resistance**

Symbol	Parameter	RS105N210I	Units	Test Conditions
RθJC	Junction-to-Case	0.63	°C/ <b>W</b>	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}$ C

## **OFF Characteristics** TJ= 25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	105			V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage			1	μΑ	VDS=80V
	Current Gate- to- Source Forward			100	•	VGS=0V VGS=20V
IGSS	Leakage Gate- to- Source Reverse				nA	VDS=0V VGS=-20V
	Leakage			-100		VDS=0V

## ON Characteristics TJ=25 °C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On- Resistance		1.9	2.5	mΩ	VGS=10V ID=20A
VGS (TH)	Gate Threshold Voltage	2.0	2.9	4.0	V	VGS=VDS ID=250μA

# Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time		26			\
trise	Rise Time		43			VDS=50V RG=3Ω
td(OFF)	Turn- OFF Delay Time		113		nS	ID=20A VGS=10V
tfall	Fall Time		64			VG3-10V



**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		10093			VGS= 0V
Coss	Output Capacitance		1559		pF	VDS=50V
Crss	Reverse Transfer Capacitance		67			f=1MHz
Qg	Total Gate Charge		160			VDS= 50V
Qgs	Gate- to- Source Charge		47		nC	ID=20A
Qgd	Gate-to-Drain(" Miller") Charge		39			VGS=10V

## **Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current			200	Α	Integral pn- diode in MOSFET
VSD	Diode Forward Voltage			1.0	V	IS=1A VGS=0V
trr	Reverse Recovery Time		100		nS	VGS=0V
Qrr	Reverse Recovery Charge		258		nC	IS=15A di/dt=100A/μs

#### Notes:

- \* 2. This single-pulse measurement was taken under TJ\_Max = 150°C
- \* 3. EAS of 1536 mJ is based on starting TJ =  $25^{\circ}$ C, L = 3.0mH, IAS = 45A, VGS = 10V, VDD = 50V; 100% test at L =0.5mH, IAS =64A
- \* 4. The power dissipation PD is based on TJ\_Max = 150°C.
- \* 5. This value is guaranteed by design hence it is not included in the production test.

<sup>\* 1.</sup> Computed continuous current assumes the condition of TJ\_Max while the actual continuous current depends on the thermal & electro-mechanical application board design



## **Typical Feature Curve**

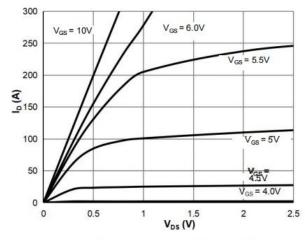


Figure 1: Saturation Characteristics

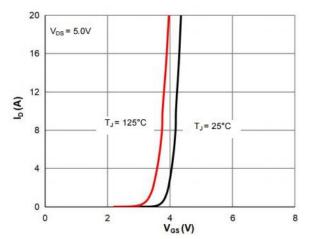


Figure 2: Transfer Characteristics

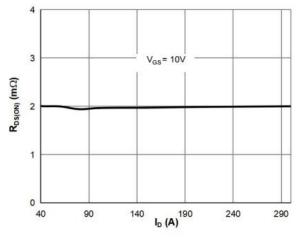


Figure 3: R<sub>DS(ON)</sub> vs. Drain Current

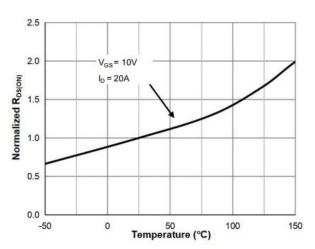


Figure 4:  $R_{DS(ON)}$  vs. Junction Temperature

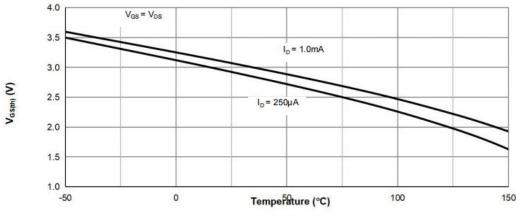
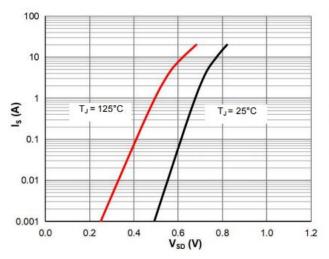


Figure 5:  $V_{GS(th)}$  vs. Junction Temperature







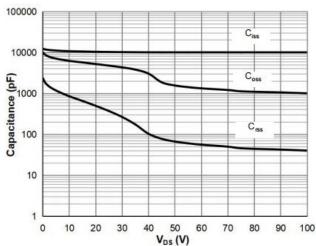


Figure 8: Capacitance Characteristics

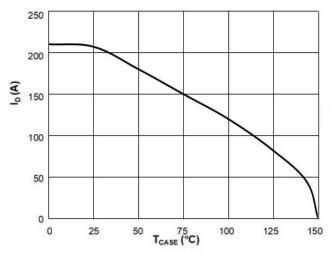


Figure 9: Current De-rating

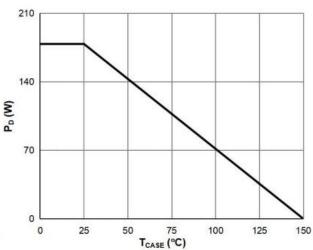


Figure 10: Power De-rating

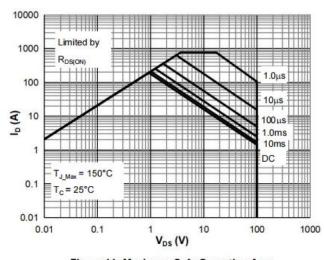


Figure 11: Maximum Safe Operating Area

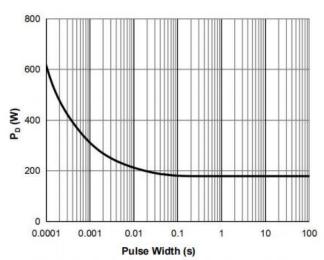


Figure 12: Single Pulse Power Rating, Junction-to-Case



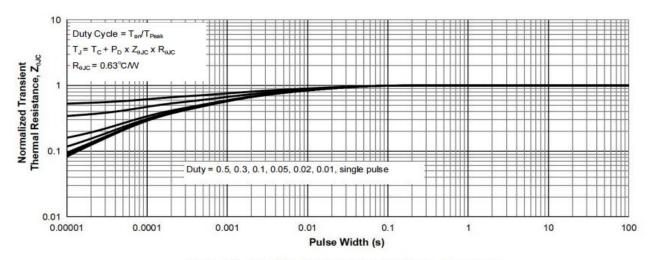
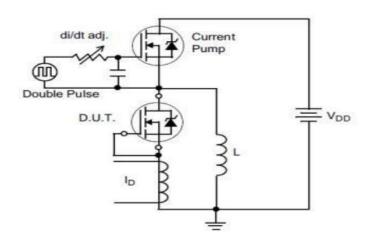


Figure 13: Normalized Maximum Transient Thermal Impedance

## **Test ircuits and Waveforms**



 $di/dt = 100A/\mu A$   $Q_{rr}$ 

Figure E.Diode Reverse Recovery Test Circuit

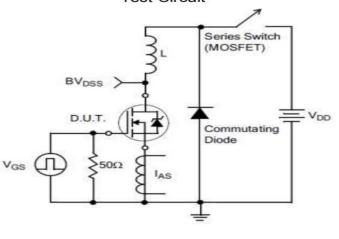


Figure F.Diode Reverse Recovery Waveform

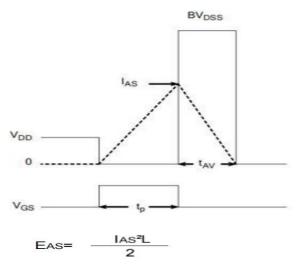
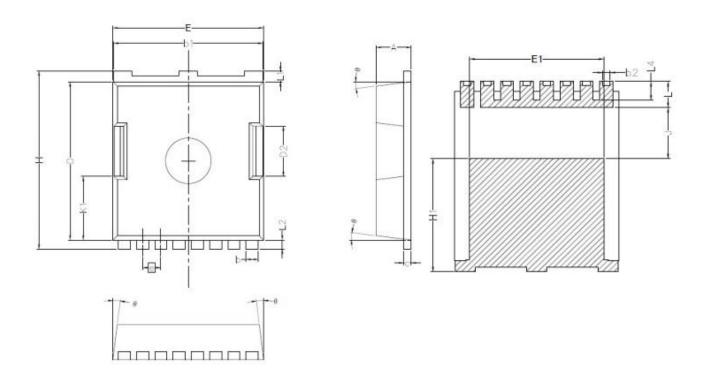


Figure G.Unclamped Inductive Switching Test Circuit

Figure H.Unclamped Inductive Switching Waveforms



# Package outline drawing(TOLL-8L Unit: mm)



Symbol	MIN. Dimension	s In Millimeters MAX.		
A	2.20	2.40		
b	0.90	0.90		
b1	9.70	9.90		
b2	0.42	0.50		
С	0.40	0.60		
D	10.28	10.58		
D2	3.10	3.50		
E	9.70	10.10		
E1	7.90	8.30		
е	1	20BSC		
Н	11.48	11.88		
H1	6.75	7.15		
N		8		
J	3.00	3.30		
K1	3.98	4.38		
L	1.40	1.80		
L1	0.60	0.80		
L2	0.50	0.70		
L4	1.00	1.30		
Θ	4°	10°		



#### **Disclaimers:**

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information in current and complete. All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale. Testing, reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement, testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using Reasunos's components. To minimize risk, customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights, nor the rights of others. Reproduction of inform- ation in Reasunos's data sheets or data books is permissible only if reproduction is without modification oralteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

### **Life Support Policy:**

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.

#### As used herein:

- 1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.
- 2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.