

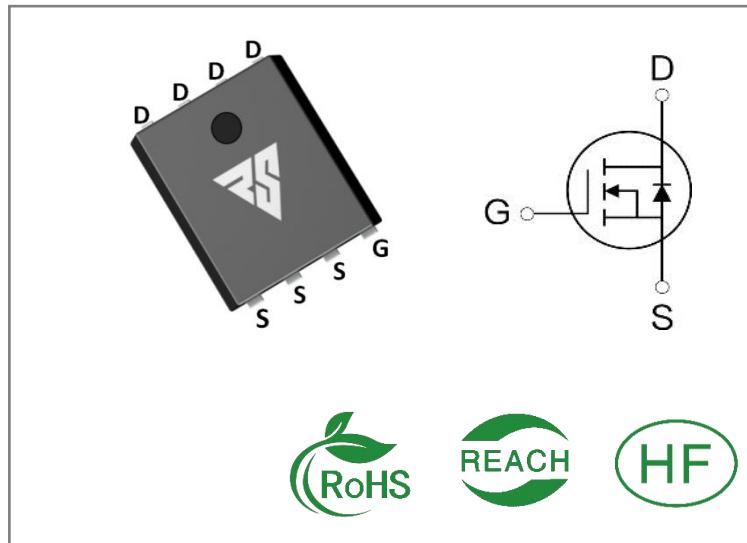
ID	R _{DS(ON)} (Typ)	V _{DSS}
130A	1.45mΩ	40V

Applications:

- Load Switch
- PWM Applications
- Power Management

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability


Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS40N130G	DFN5*6	RS40N130G	Tape&reel	5000 PCS

Absolute Maximum Ratings T_c= 25°C unless otherwise specified

Symbol	Parameter	RS40N130G	Units
V _{DSS}	Drain-to-Source Voltage	40	V
ID	Continuous Drain Current TC=25°C	130	A
ID	Continuous Drain Current TC=100°C	82	
IDM	Pulsed Drain Current (Note*1)	390	
PD	Power Dissipation	115	W
V _{GS}	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy L = 3mH, V _{DD} = 25V, R _G = 25 Ω, T _C =25°C	720	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
T _J and T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS40N130G	Units	Test Conditions
R _{θJC}	Junction-to-Case	0.9	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 150 °C
R _{θJA}	Junction-to-Ambient	40		1 cubic foot chamber, free air.

OFF Characteristics TJ= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	40	--	--	V	VGS=0V, ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=40V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V ,VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance (Note*2)	--	1.45	1.75	mΩ	VGS=10V, ID=20A
		--	1.9	2.5	mΩ	VGS=4.5V, ID=20A
VGS(TH)	Gate Threshold Voltage	1	--	2.5	V	VGS=VDS, ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	18.8	--	nS	VDS=20V ID=20A RG=2.2Ω VGS=10V
trise	Rise Time	--	70.1	--		
td(OFF)	Turn- OFF Delay Time	--	136.8	--		
tfall	Fall Time	--	92.3	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C _{iss}	Input Capacitance	--	7100	--	pF	V _{GS} =0V V _{DS} =25V f=1MHz
C _{oss}	Output Capacitance	--	1298	--		
C _{rss}	Reverse Transfer Capacitance	--	55	--		
Q _g	Total Gate Charge	--	132	--	nC	V _{DS} =20V I _D =20A V _{GS} =10V
Q _{gs}	Gate- to- Source Charge	--	25	--		
Q _{gd}	Gate-to-Drain(" Miller") Charge	--	24.6	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current	--	--	130	A	Integral pn- diode in MOSFET
I _{SM}	Maximum Pulsed Current	--	--	390	A	
V _{SD}	Diode Forward Voltage	--	--	1.3	V	I _S =20A,V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	56	--	nS	I _S =20A di/dt=100A/μs
Q _{rr}	Reverse Recovery Charge	--	54	--	nC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

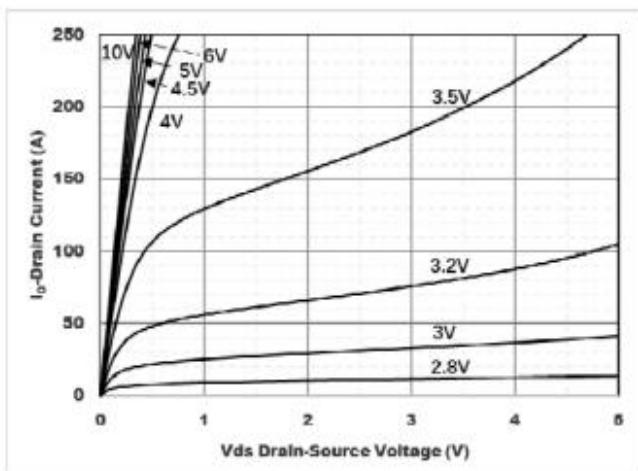


Figure1. Output Characteristics

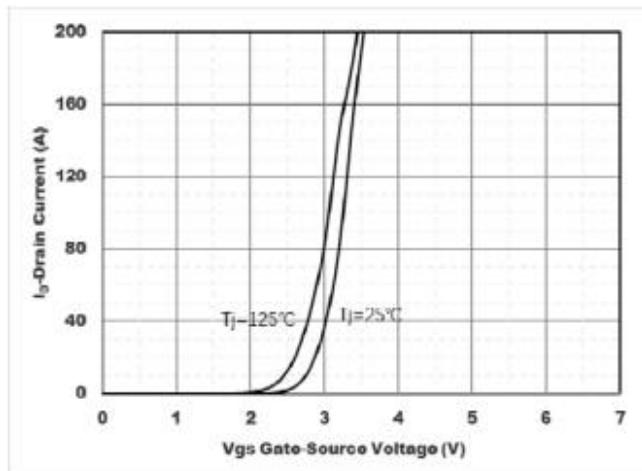


Figure2. Transfer Characteristics

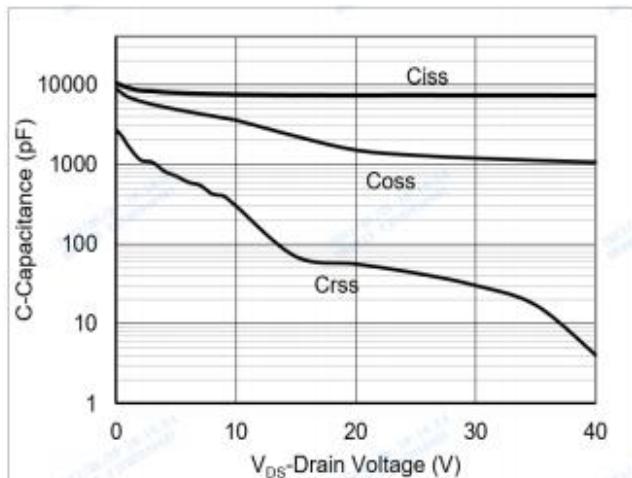


Figure3. Capacitance Characteristics

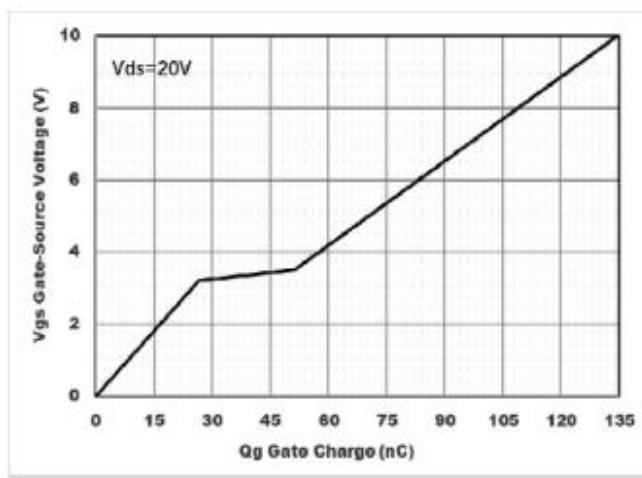


Figure4. Gate Charge

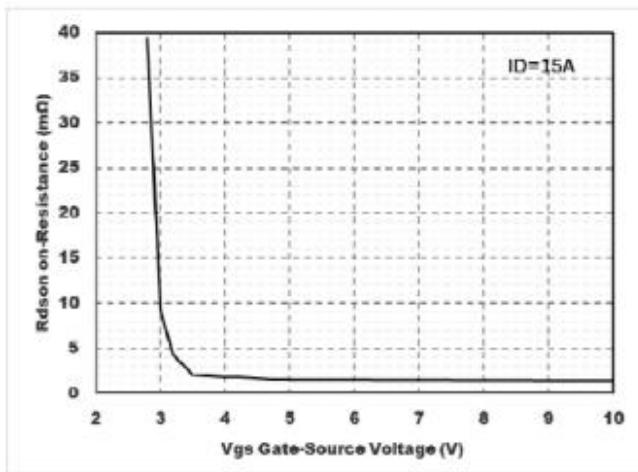


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

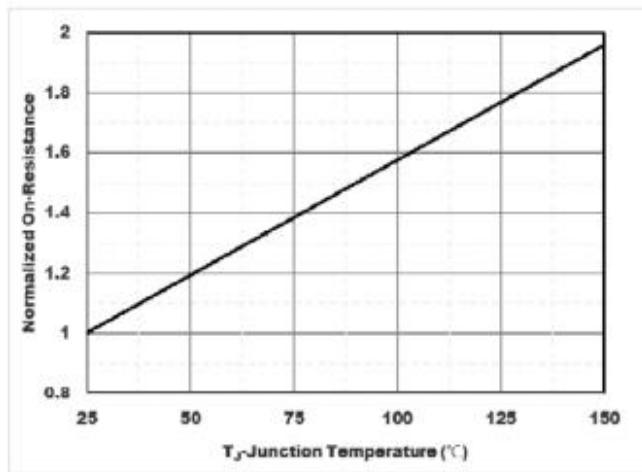


Figure6.Normalized On-Resistance

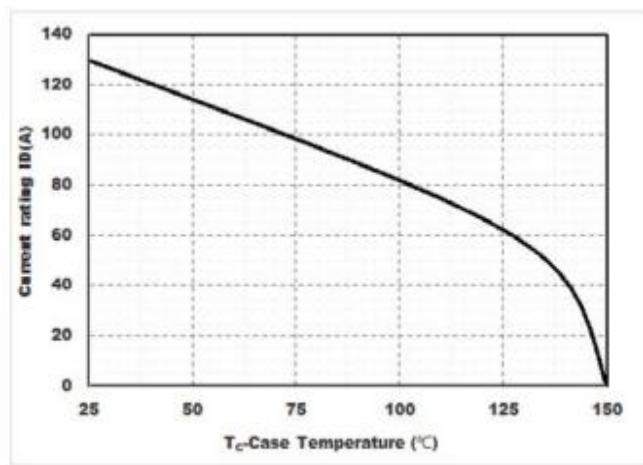


Figure7. Drain current

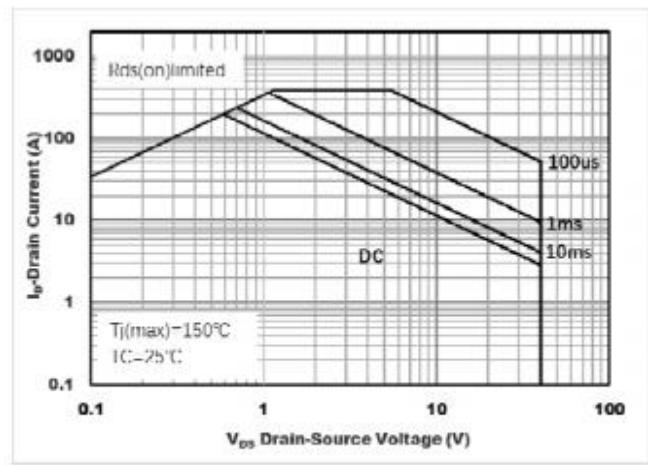


Figure8.Safe Operation Area

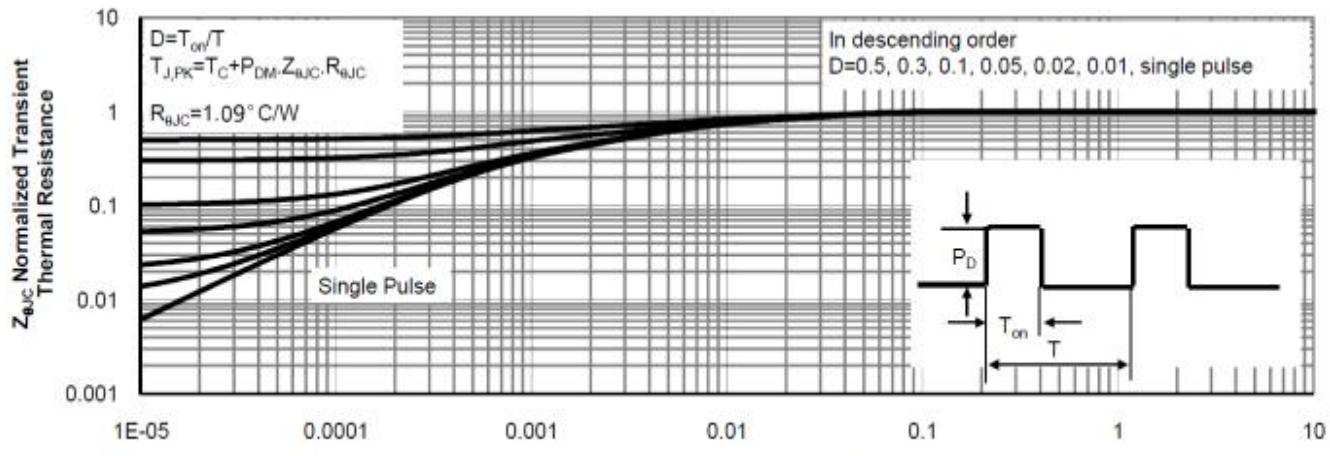


Figure9.Normalized Maximum Transient thermal impedance

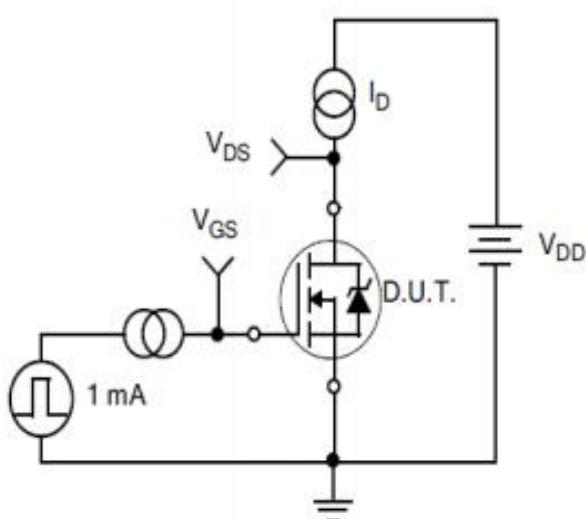
Test Circuits and Waveforms


Figure A.
Gate Charge Test Circuit

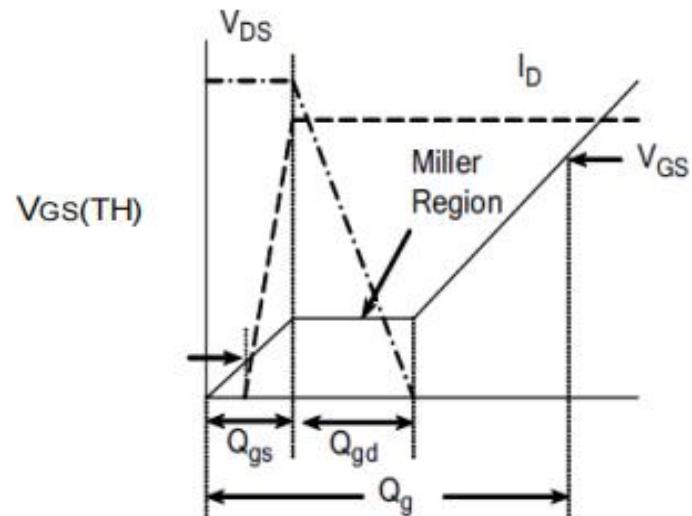


Figure B.
Gate Charge Waveform

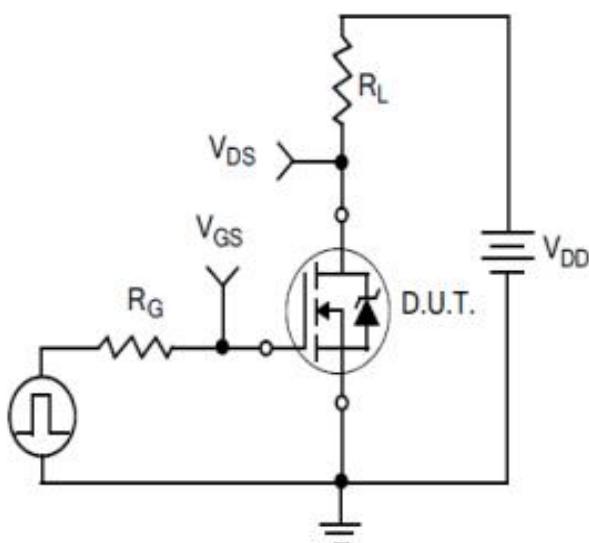


Figure C.
Resistive Switching Test Circuit

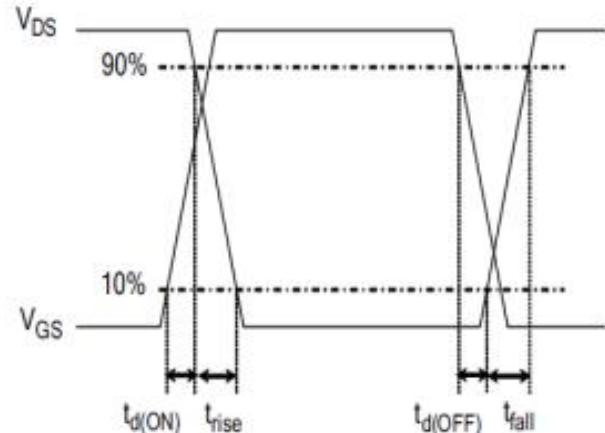


Figure D.
Resistive Switching Waveforms

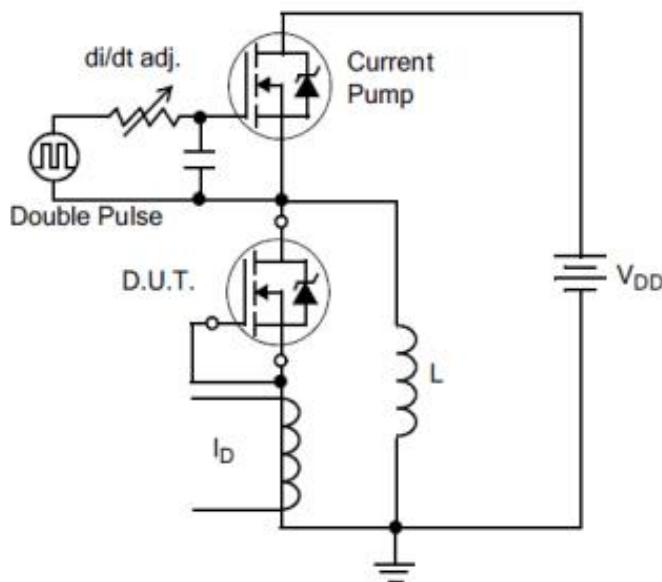
Test Circuits and Waveforms


Figure E. Diode Reverse Recovery Test Circuit

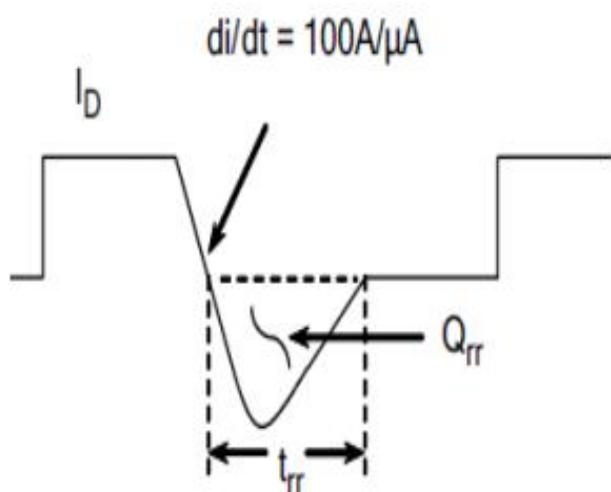


Figure F. Diode Reverse Recovery Waveform

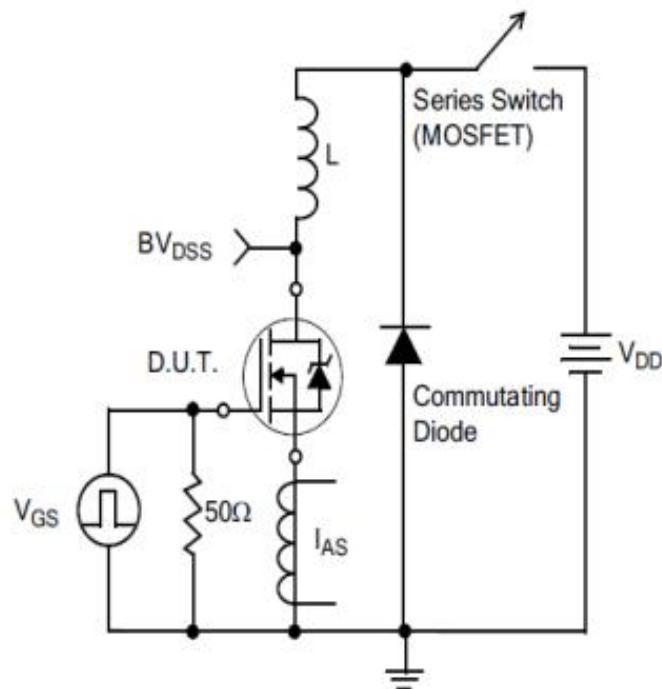
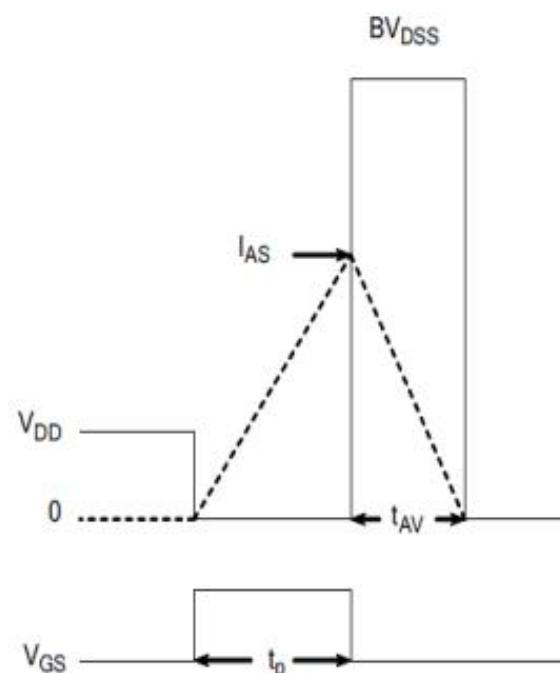
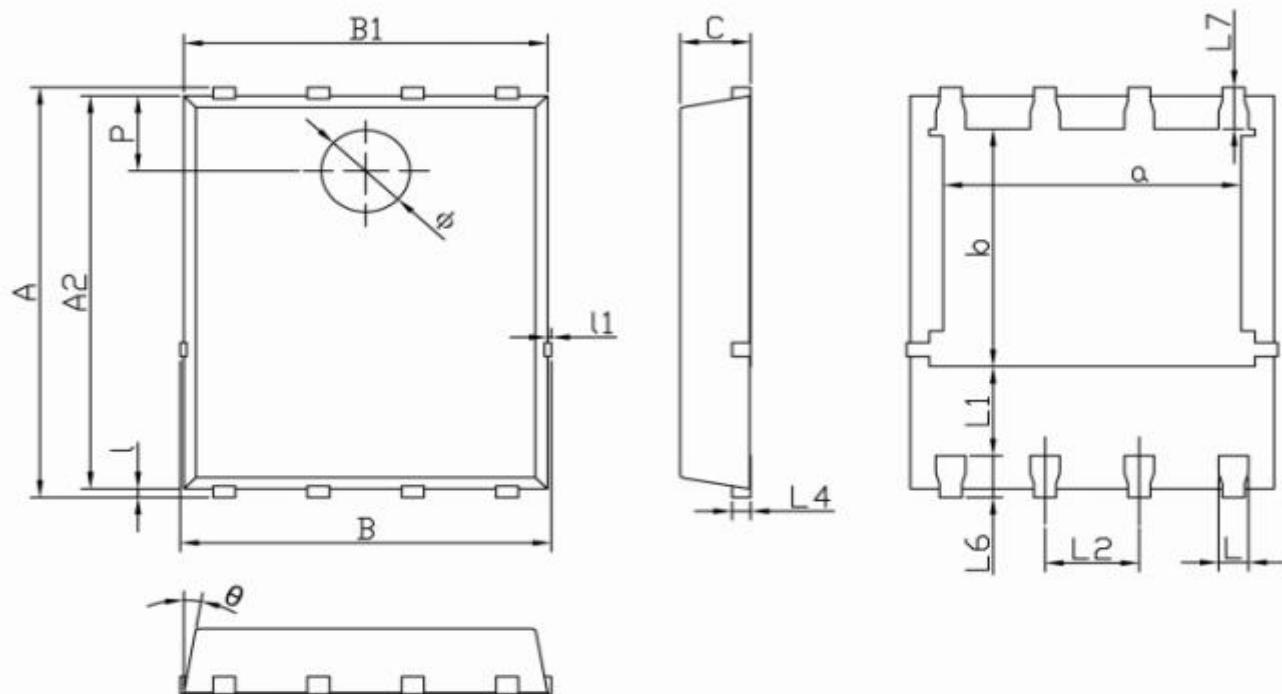


Figure G. Unclamped Inductive Switching Test Circuit



$$EAS = \frac{I_{AS}^2 L}{2}$$

Figure H. Unclamped Inductive Switching Waveforms

Package outline drawing(DFN5*6 Unit: mm)


Dimensions In Millimeterer			
Symbol	MIN	TYP	MAX
A	5.90	6.00	6.10
α	3.91	4.01	4.11
A2	5.70	5.75	5.80
B	4.90	5.00	5.10
b	3.37	3.47	3.57
B1	4.80	4.90	5.00
C	0.90	0.95	1.00
L	0.35	0.40	0.45
l	0.06	0.13	0.20
L1	1.10	-	-
l1	-	-	0.10
L2	1.17	1.27	1.37
L4	0.21	0.26	0.34
L6	0.51	0.61	0.71
L7	0.51	0.61	0.71
P	1.00	1.10	1.20
θ	8°	10°	12°
Φ	1.10	1.20	1.30

Disclaimers:

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the specifications at the time of sale. Testing, reliability and quality control are used to the extent Reasunos deems necessary to support this warranty. Except where agreed upon by contract, actual agreement, testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using Reasunos's components. To minimize risk, customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in Reasunos's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsible or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all express or implied warranties for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsible or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
 - a. are intended for surgical implant into the human body,
 - b. support or sustain life,
 - c. whose failure to when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.