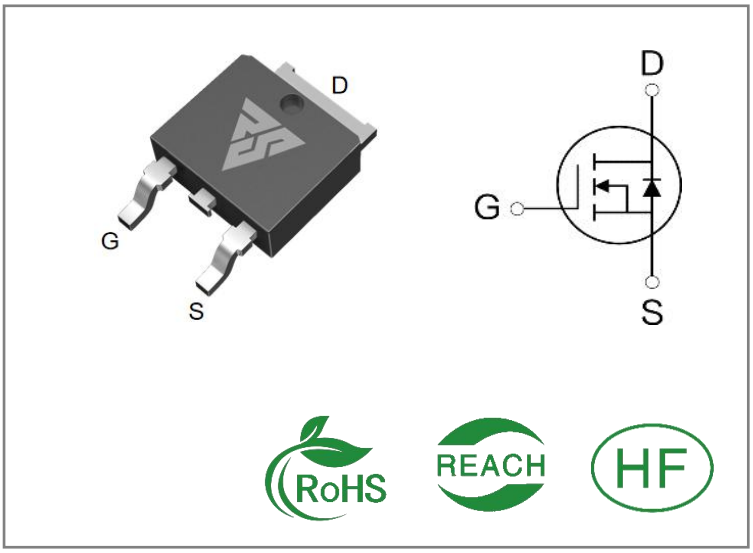
ID	R_{DS}(ON)(Typ)	VDSS
4A	880mΩ	650V



Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC-DC Switching Power Supply

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSU4N65D	T0-252	RSU4N65D	Tape&reel	2500 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RSU4N65D	Units
VDSS	Drain-to-Source Voltage	650	V
ID	Continuous Drain Current TC=25℃	4	A
ID	Continuous Drain Current TC=100℃	2.5	
IDM	Pulsed Drain Current (Note*1)	12	
PD	Power Dissipation	37	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=10mH,VDS= 50V, RG = 25Ω，TC=25℃	80	mJ
dv/dt	MOSFET dv/ dt ruggednessVDS = 0...400V	50	V/ns
dv/dt	Reverse diode dv/dt VDS = 0...400V, Tj = 25℃, ISD≤ID	15	V/ns
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RSU4N65D	Units	Test Conditions
RθJC	Junction-to-Case	3.4	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	62		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650	--	--	V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=650V,VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	880	1000	mΩ	VGS=10V,ID=2A
VGS(TH)	Gate Threshold Voltage	2.5	--	4	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	35	--	nS	VDS=400V ID=2A RG=25Ω
trise	Rise Time	--	8	--		
td(OFF)	Turn- OFF Delay Time	--	62	--		
tfall	Fall Time	--	19	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	284	--	pF	VGS=0V VDS=100V f=1MHz
Coss	Output Capacitance	--	21	--		
Crss	Reverse Transfer Capacitance	--	9.5	--		
Qg	Total Gate Charge	--	8.7	--	nC	VDS=520V ID=2A VGS=10V
Qgs	Gate- to- Source Charge	--	1.2	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	3.7	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	4	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	12	A	
VSD	Diode Forward Voltage	--	0.85	1.2	V	IS=2A,VGS=0V
trr	Reverse Recovery Time	--	112	--	nS	VR=50V IS=2A,di/dt=100A /μs
Qrr	Reverse Recovery Charge	--	0.51	--	μC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

Figure 1. Output Characteristics

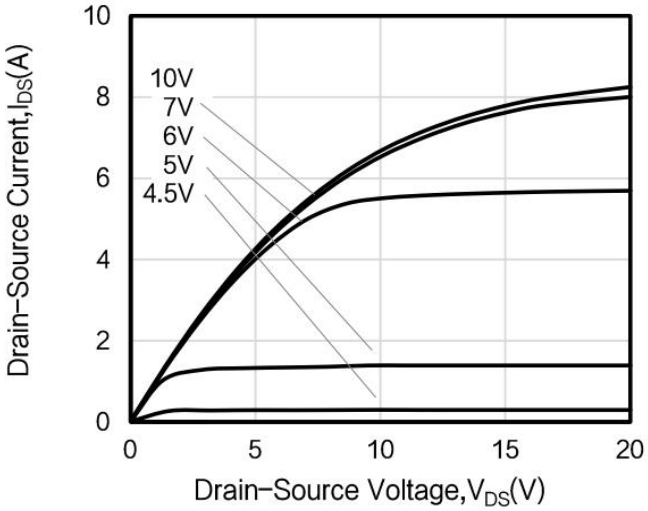


Figure 2. Transfer Characteristics

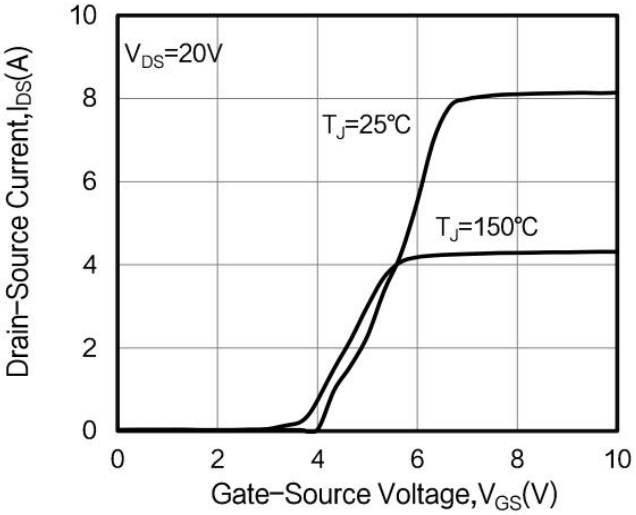


Fig.3 On−Resistance vs.Drain Current for Various T_j

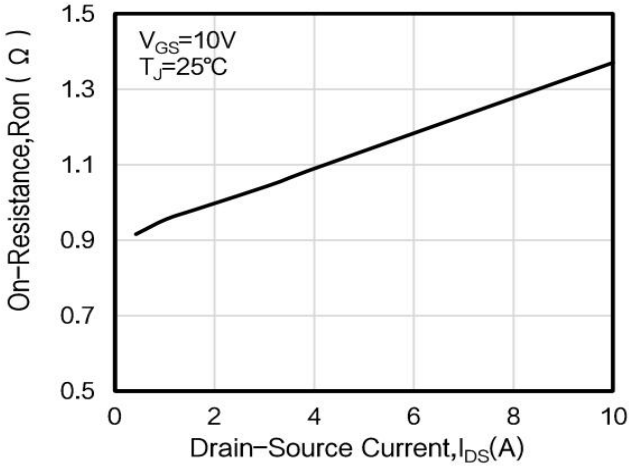


Fig.4 Capacitances

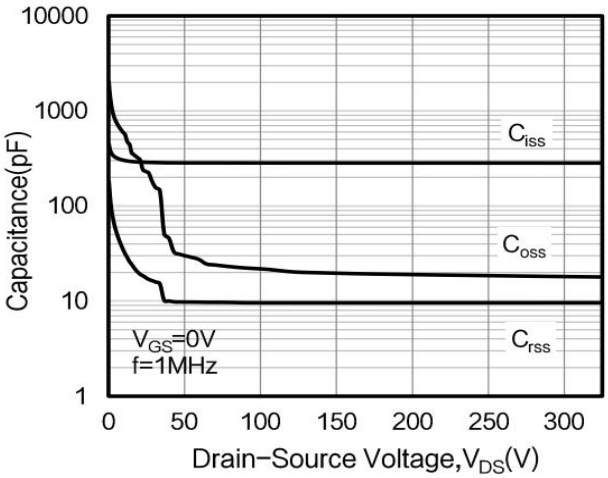


Figure 5. Gate Charge

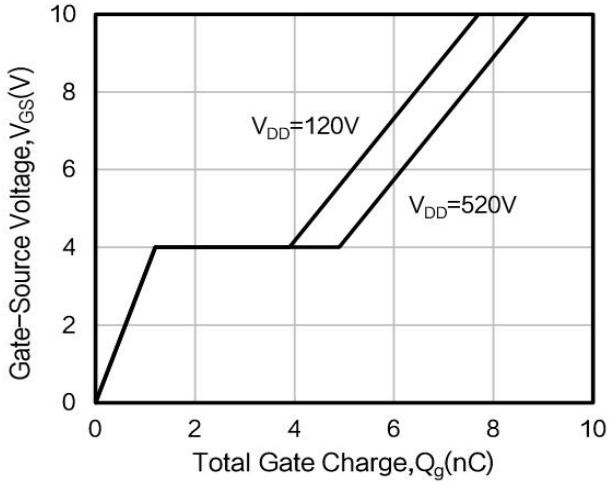


Figure 6. Body Diode Forward Voltage

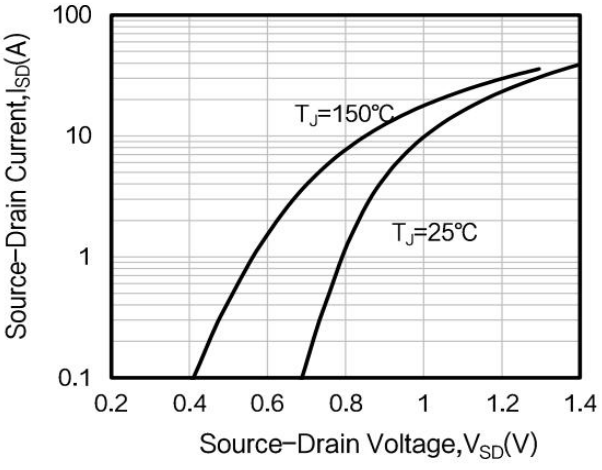


Fig.7 Normalized On-Resistance vs. Temperature

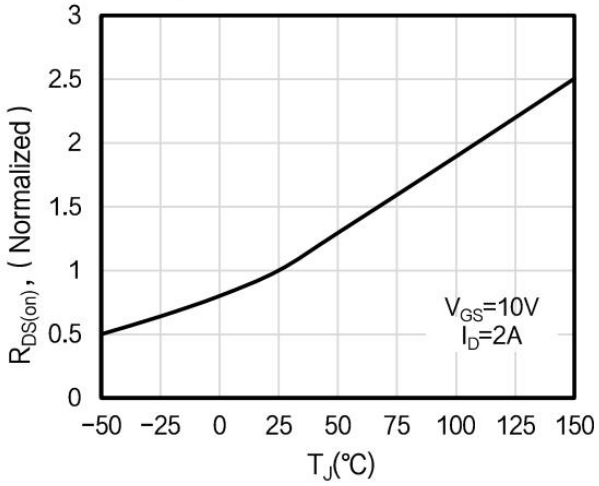


Fig.8 Normalized Threshold Voltage vs. Temperature

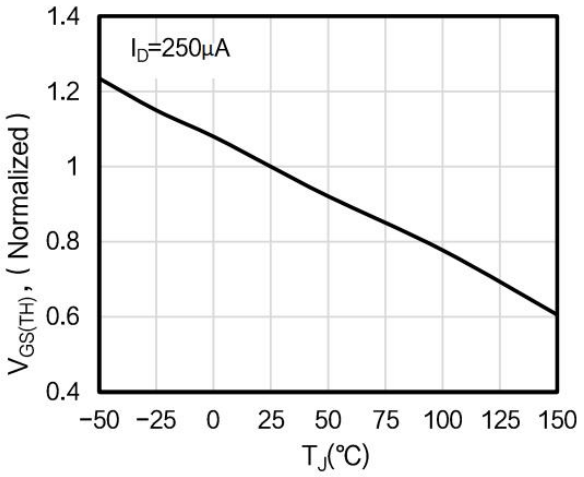


Figure 9. Transient Thermal Impedance

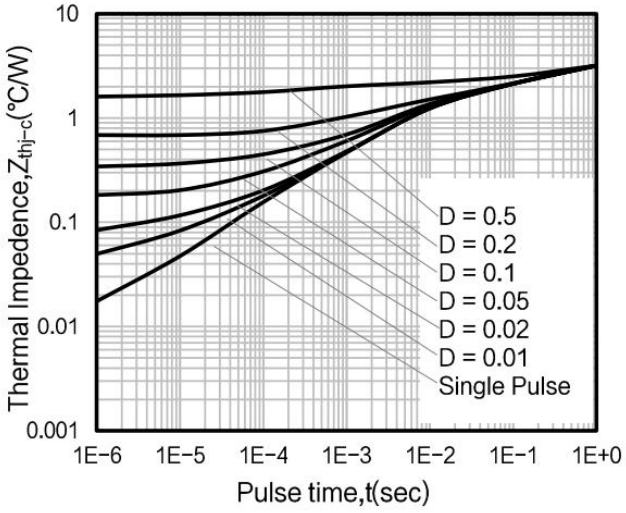
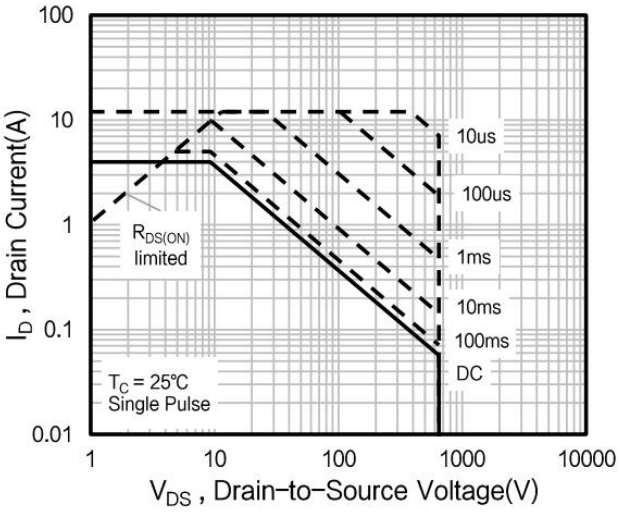


Figure 10. Safe Operation Area



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

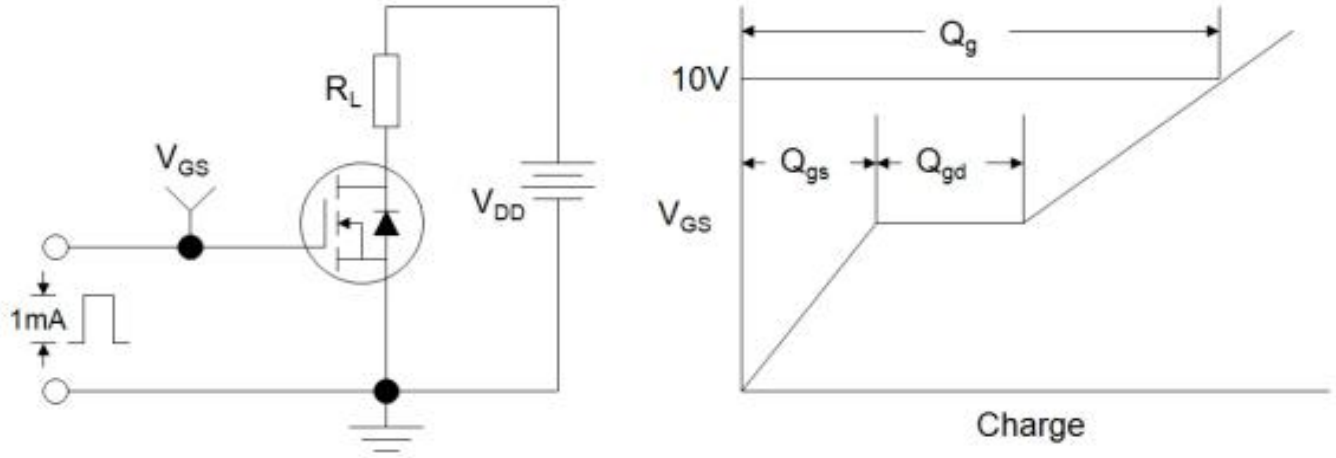


Figure B: Resistive Switching Test Circuit and Waveform

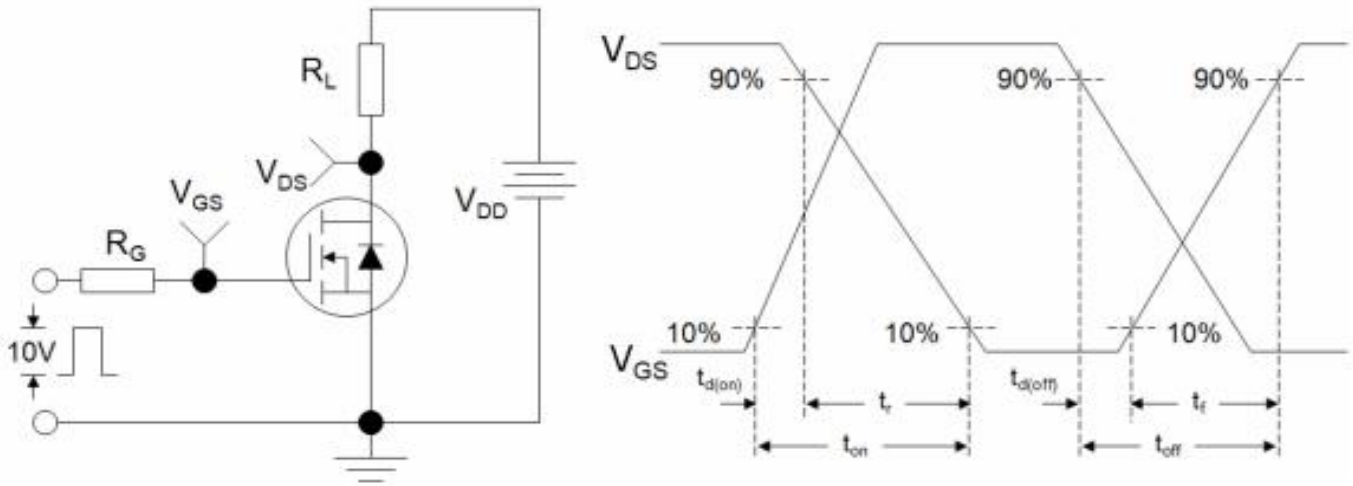
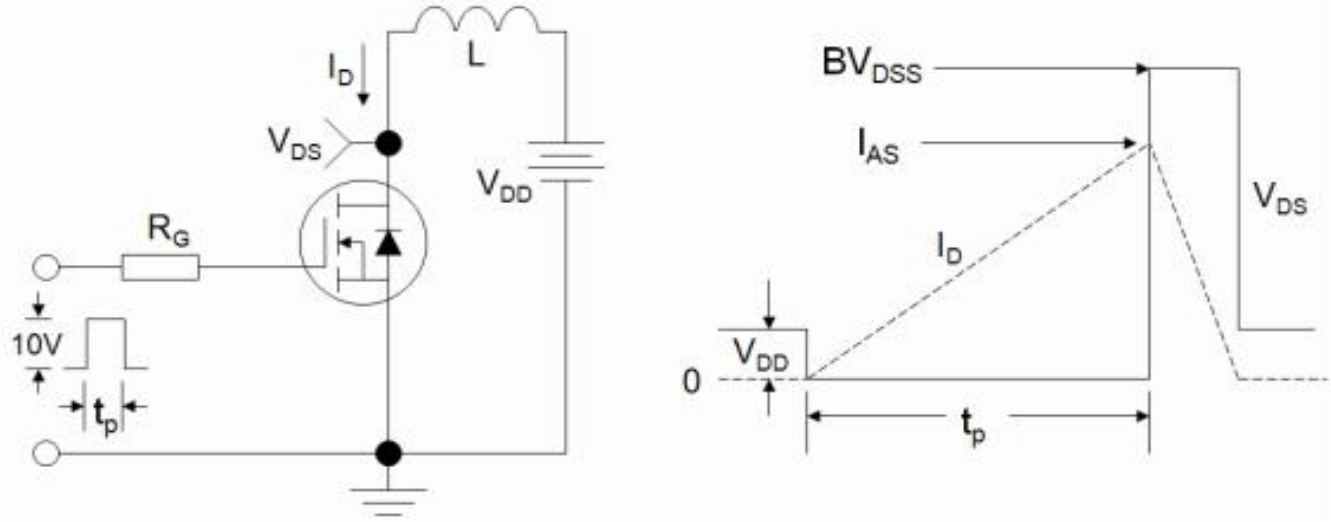
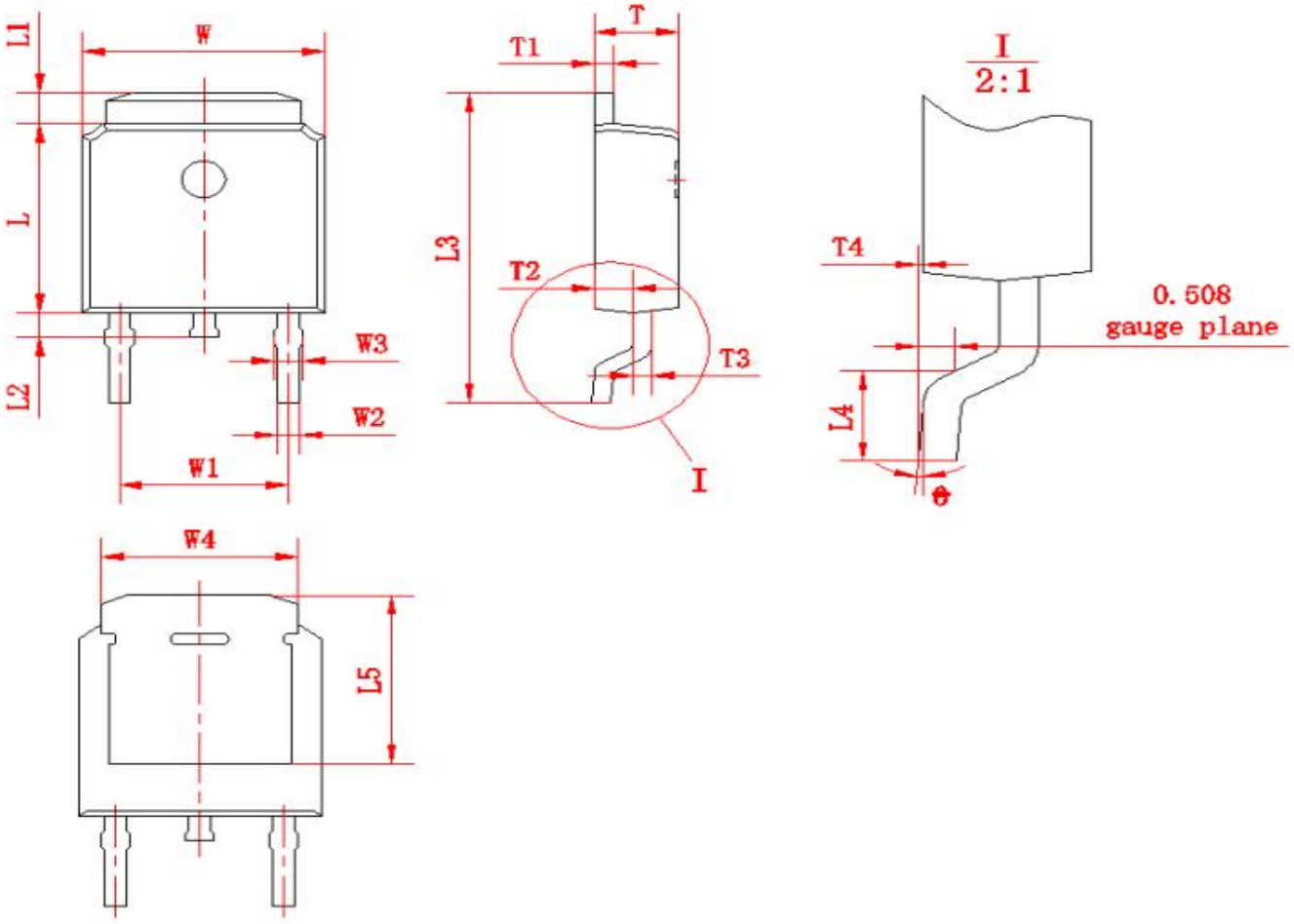


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		θ	0	8
L	6.00	6.20	T	2.20	2.40			

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