

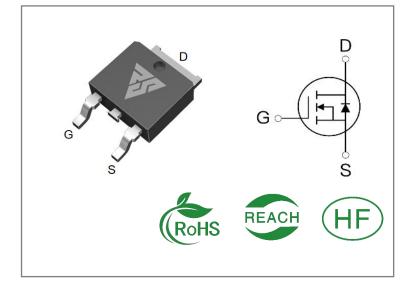
ID	R _{DS} (ON)(Typ)	VDSS
13.8A	240mΩ	650V

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC-DC Switching Power Supply

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability



Ordering Information

Part Number	Package	Package Marking		Qty.	
RS65R280D	T0-252	RS65R280D	Tape&reel	2500 PCS	

Absolute Maximun Ratings Tc= 25℃ unless otherwise specified

Symbol	Parameter	RS65R280D	Units	
VDSS	Drain-to-Source Voltage	650	V	
ID	Continuous Drain Current TC=25℃	13.8		
ID	Continuous Drain Current TC=100℃	8.7	A	
IDM	Pulsed Drain Current (Note*1)	42		
PD	Power Dissipation	75	W	
VGS	VGS Gate- to- Source Voltage		V	
EAS	Single Pulse Avalanche Engergy L=10mH,VDS= 50V, RG = 25 Ω , TC=25 $^{\circ}$ C	260	mJ	
dv/dt	MOSFET dv/ dt ruggedness VDS = 0400V	50	V/ns	
dv/dt	Reverse diode dv/dt VDS = 0400V, Tj = 25°C, ISD≤ID	15	V/ns	
	Maximum Temperature for Soldering	300		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	\mathbb{C}	
TJ and TSTG	and Operating Junction and Storage			

^{*} Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the" Absolute Maximum Ratings" Table may cause permanent damage to the device.



Thermal Resistance

Symbol	Parameter	RS65R280D	Units	Test Conditions
RθJC	Junction-to-Case	0.9	°C/W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\mathrm{C}$
RθJA	Junction-to- Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25 °C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650			٧	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current		1	1	μΑ	VDS=650V,VGS=0 V
IGSS	Gate- to- Source Forward Leakage			100	nA	VGS=30V ,VDS=0V
	Gate- to- Source Reverse Leakage			100		VGS=-30V ,VDS=0 V

ON Characteristics TJ=25 °C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On- Resistance(Note*2)		240	280	mΩ	VGS=10V,ID=4.5A
VGS(TH)	Gate Threshold Voltage	2		4	V	VGS=VDS,ID=250μ A

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time		24			
trise	Rise Time		41			VDS=325V
td(OFF)	Turn- OFF Delay Time		86		nS	ID=13.8A RG=25Ω
tfall	Fall Time		37			



Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		989			VGS=0V
Coss	Output Capacitance		73		pF	VDS=50V
Crss	Reverse Transfer Capacitance		4.4			f=1.0MHz
Qg	Total Gate Charge		26			VDS=520V
Qgs	Gate- to- Source Charge		4.9		nC	ID=13.8A
Qgd	Gate-to-Drain(" Miller") Charge		12			VGS=10V

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current			13.8	Α	Integral pn- diode
ISM	Maximum Pulsed Current			42	Α	in MOSFET
VSD	Diode Forward Voltage			1.4	٧	IS=13.8A,VGS=0V
trr	Reverse Recovery Time		302		nS	VR=100V
Qrr	Reverse Recovery Charge		3.7		μС	IS=13.8A,di/dt=100 A/μs

Notes:

^{* 1.} Repetitive rating, pulse width limited by maximum junction temperature.

^{* 2.} Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%



Typical Feature Curve

Figure 1. Output Characteristics

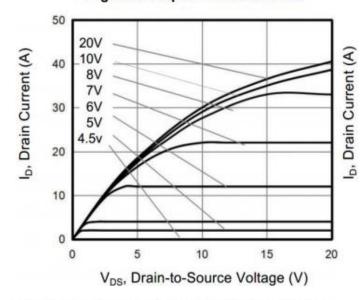


Figure 3. On-Resistance VS.Drain Current

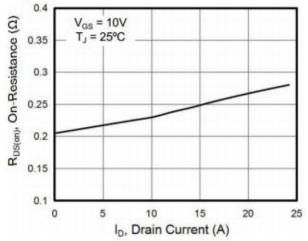


Figure 5. Gate Charge

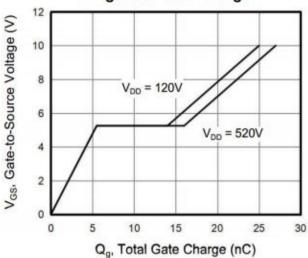


Figure 2. Transfer Characteristics

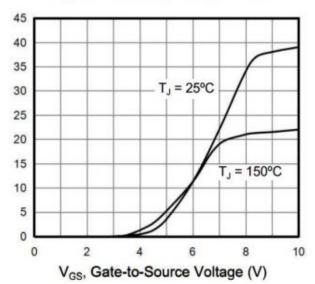


Figure 4. Capacitance

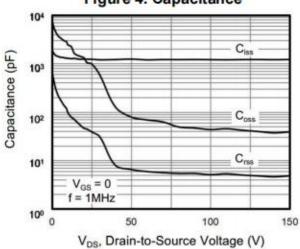
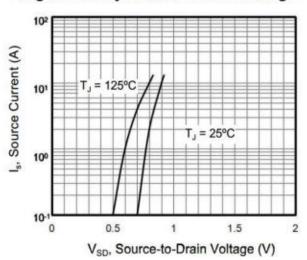


Figure 6.Body Diode Forward Voltage



REV:P-B01-03-2024 www.reasunos.com



Figure 7.On-Resistan ce vs. Junction Temperature

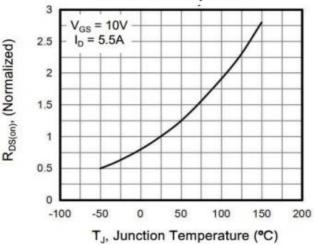


Figure 9.Breakdown voltage vs.
Junction Temperature

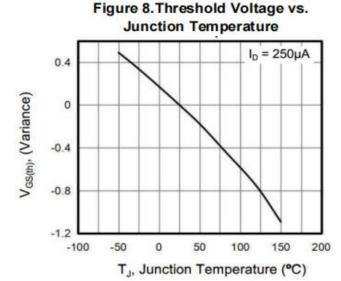


Figure 10.Transient Thermal Impedance

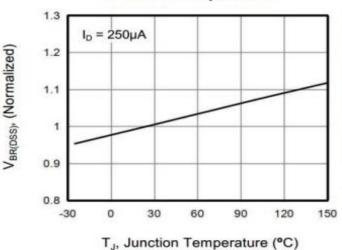
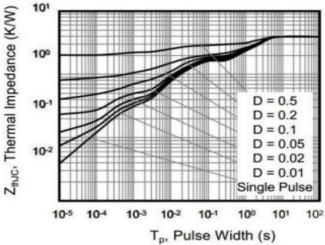
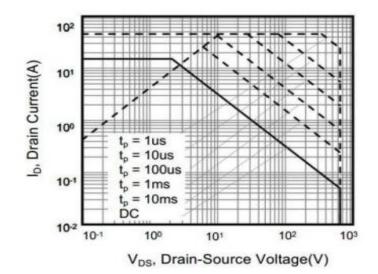


Figure 11.Safe operation area for





Copyright Reasunos



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

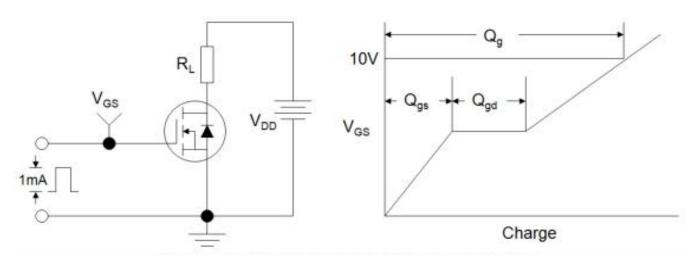


Figure B: Resistive Switching Test Circuit and Waveform

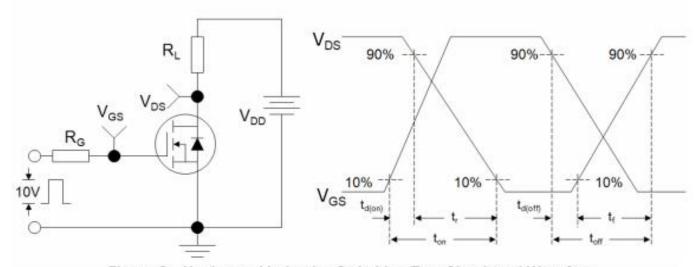
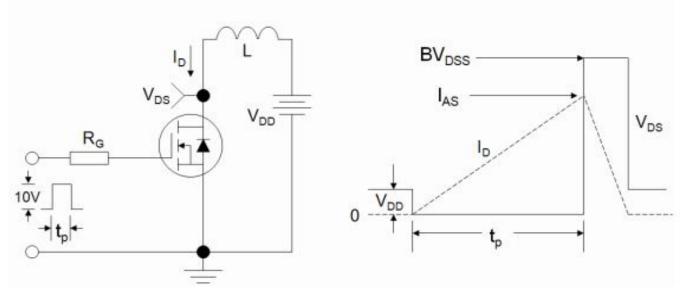


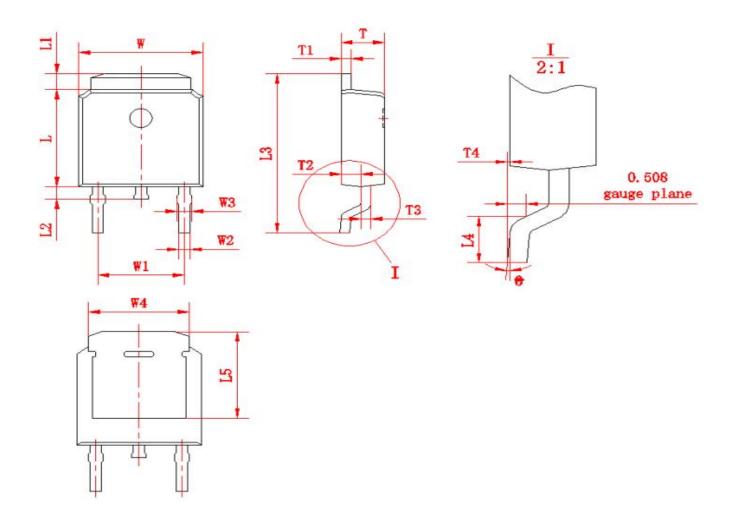
Figure C: Unclamped Inductive Switching Test Circuit and Waveform



REV:P-B01-03-2024 www.reasunos.com 6 / 8



Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
小 万	Min	Max	17 5	Min	Max	१५ ५	Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.5	572)	L2	0.60 1.00		T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	Т3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5	.3)	L5	(5.20)		0	0	8
L	6.00	6.20	Т	2.20	2.40			



Disclaimers:

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information in current and complete. All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale. Testing, reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement, testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using Reasunos's components. To minimize risk, customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights, nor the rights of others. Reproduction of inform- ation in Reasunos's data sheets or data books is permissible only if reproduction is without modification oralteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as cri- tical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.

As used herein:

- 1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,
- c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.