

ID	$R_{DS(ON)}$ (Typ)	VDSS
7A	740mΩ	800V

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC-DC Switching Power Supply

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability
- Built-in ESD Diode

Ordering Information

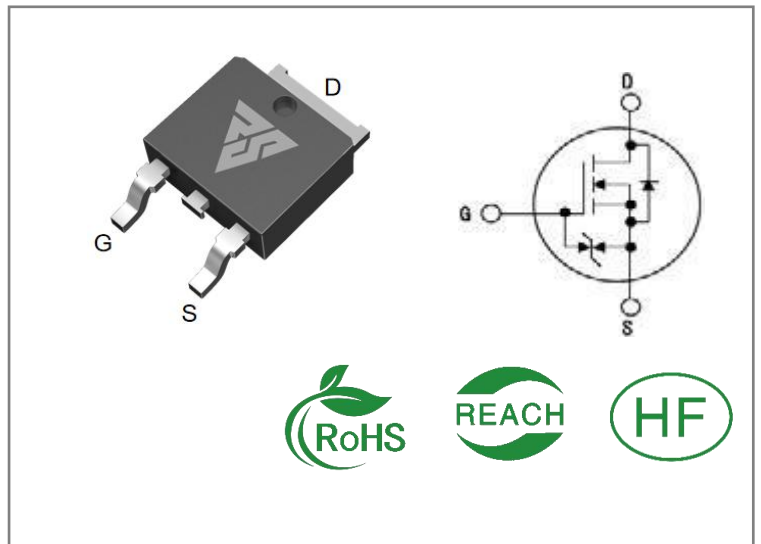
Part Number	Package	Marking	Packing	Qty.
RSE80R850D	T0-252	RSE80R850D	Tape&reel	2500 PCS

Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	RSE80R850D	Units
VDSS	Drain-to-Source Voltage	800	V
ID	Continuous Drain Current $T_C = 25^\circ\text{C}$	7	A
ID	Continuous Drain Current $T_C = 100^\circ\text{C}$	4.2	
IDM	Pulsed Drain Current (Note*1)	21	
PD	Power Dissipation	66	W
VGS	Gate- to- Source Voltage	± 20	V
EAS	Single Pulse Avalanche Energy $I_{AS} = 1.4\text{A}, V_{DD} = 50\text{V}, R_G = 25\ \Omega, T_C = 25^\circ\text{C}$	84	mJ
dv/dt	MOSFET dv/ dt ruggedness $V_{DS} = 0 \dots 400\text{V}$	50	V/ns
dv/dt	Reverse diode dv/dt $V_{DS} = 0 \dots 400\text{V}, T_j = 25^\circ\text{C}, I_{SD} \leq I_D$	15	V/ns
VESD(G-S)	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000	V
TL TPKG	Maximum Temperature for Soldering	300	$^\circ\text{C}$
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.



Thermal Resistance

Symbol	Parameter	RSE80R850D	Units	Test Conditions
R θ JC	Junction-to-Case	1.9	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 °C
R θ JA	Junction-to- Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics T_J= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	800	--	--	V	VGS=0V,ID=1mA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=800V,VGS=0 V
IGSS	Gate- to- Source Forward Leakage	--	--	1	μA	VGS=20V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-1		VGS=-20V ,VDS=0 V

ON Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	740	850	mΩ	VGS=10V,ID=1.6A
VGS(TH)	Gate Threshold Voltage	2	--	4	V	VGS=VDS,ID=220μ A

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	23	--	nS	VDS=400V ID=2.8A RG=25Ω
trise	Rise Time	--	18	--		
td(OFF)	Turn- OFF Delay Time	--	74	--		
tfall	Fall Time	--	17	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	635	--	pF	VGS=0V VDS=500V f=1.0MHz
Coss	Output Capacitance	--	14.6	--		
Crss	Reverse Transfer Capacitance	--	2.5	--		
Qg	Total Gate Charge	--	13.7	--	nC	VDS=640V ID=2.8A VGS=10V
Qgs	Gate- to- Source Charge	--	2.9	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	4.2	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	7	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	21	A	
VSD	Diode Forward Voltage	--	--	1.3	V	IS=2.8A,VGS=0V
trr	Reverse Recovery Time	--	170	--	nS	VR=400V IS=2.8A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	1.1	--	μC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

Typical Feature Curve

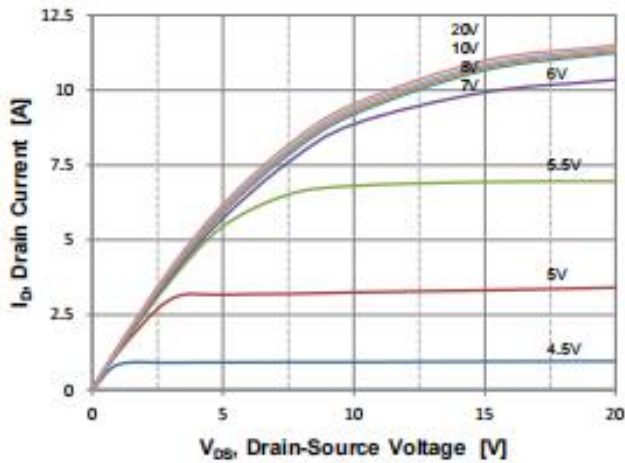


Figure 1. On Region Characteristics

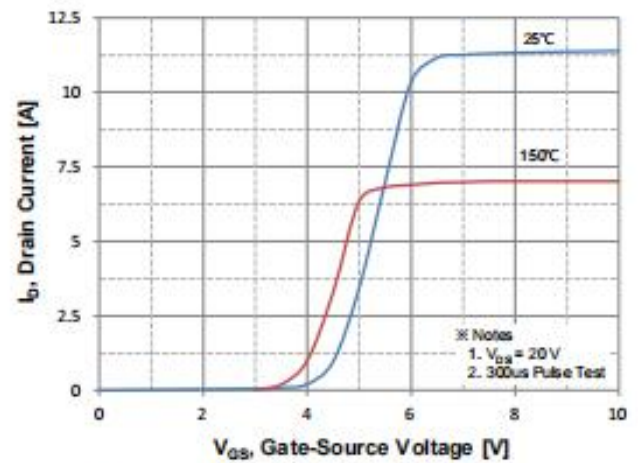


Figure 2. Transfer Characteristics

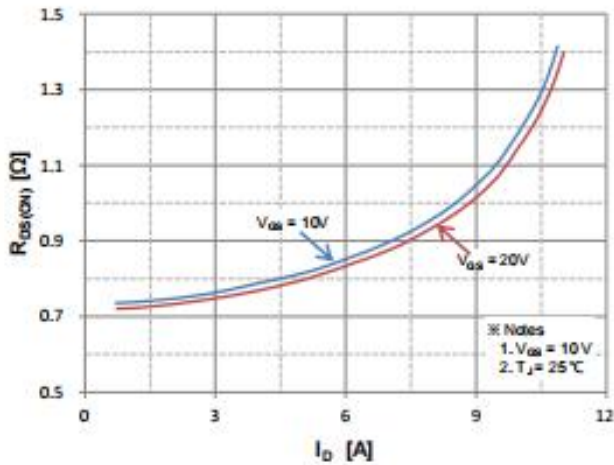


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

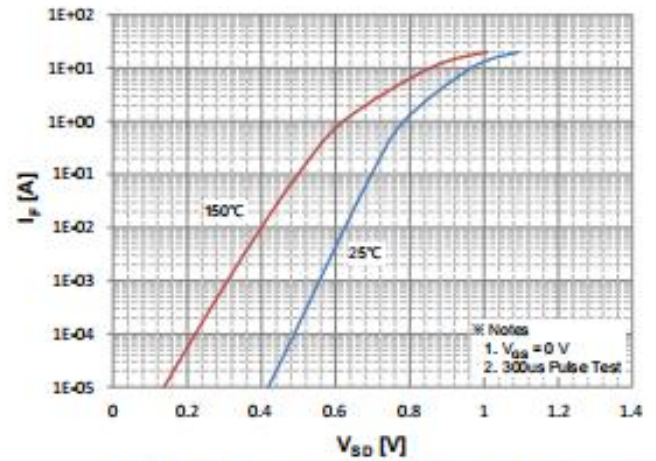


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

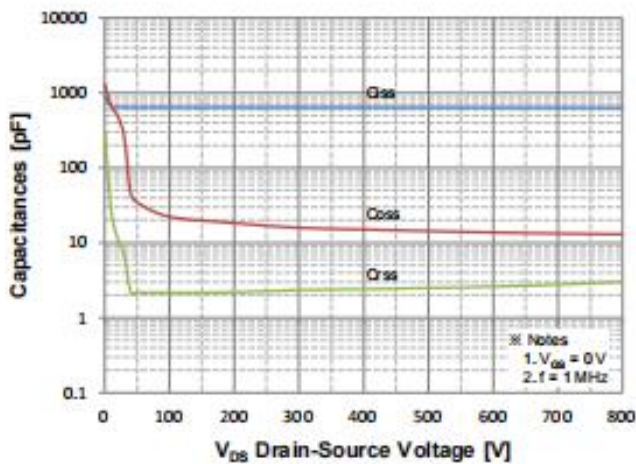


Figure 5. Capacitance Characteristics

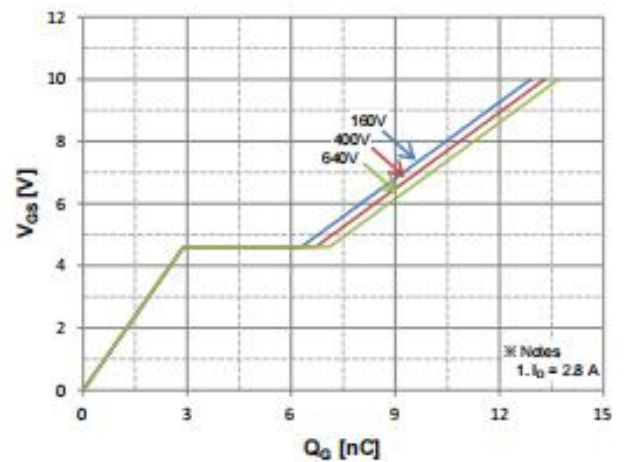


Figure 6. Gate Charge Characteristics

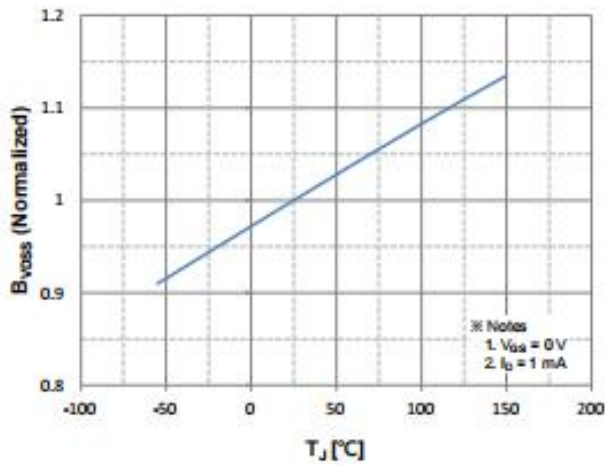


Figure 7. Breakdown Voltage Variation vs. Temperature

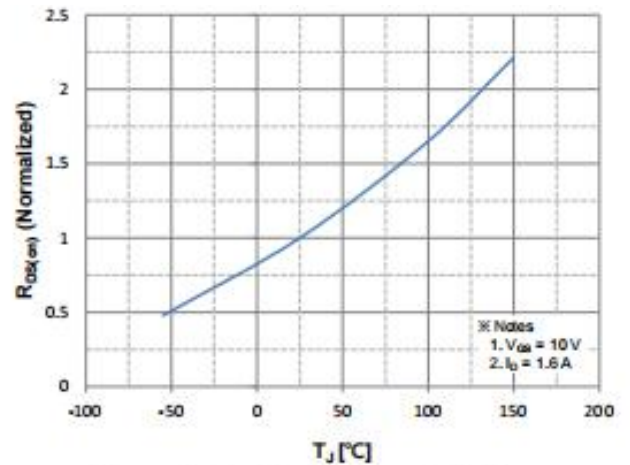


Figure 8. On-Resistance Variation vs. Temperature

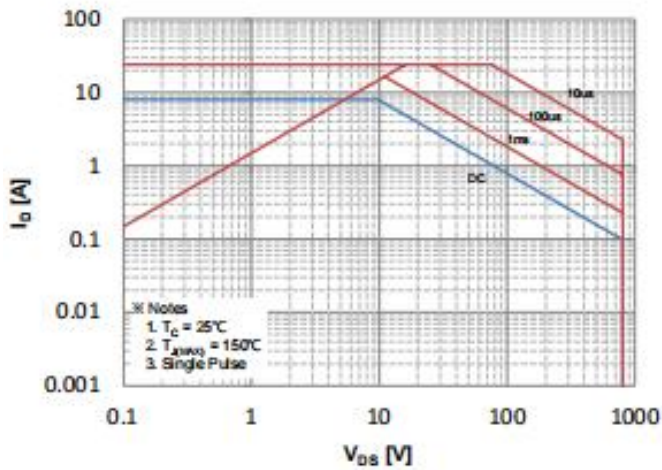


Figure 9. Maximum Safe Operating Area

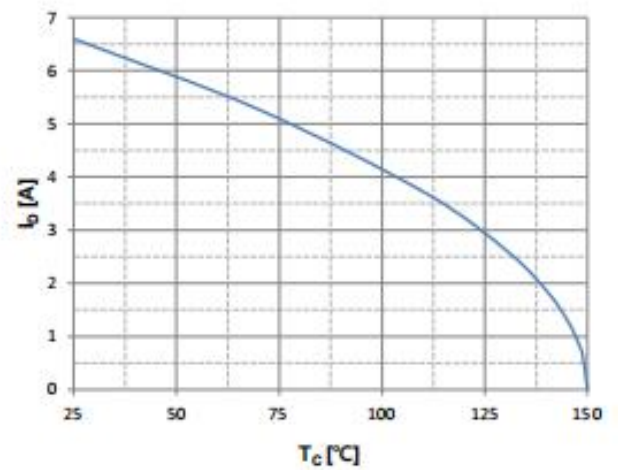


Figure 10. Maximum Drain Current vs. Case Temperature

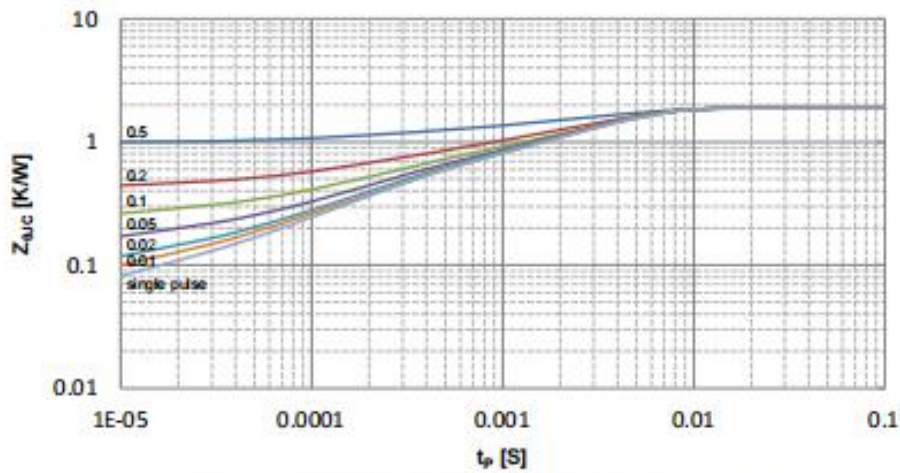


Figure 11. Transient Thermal Response Curve

Test Circuits and Waveforms

Fig 12. Gate Charge Test Circuit & Waveform

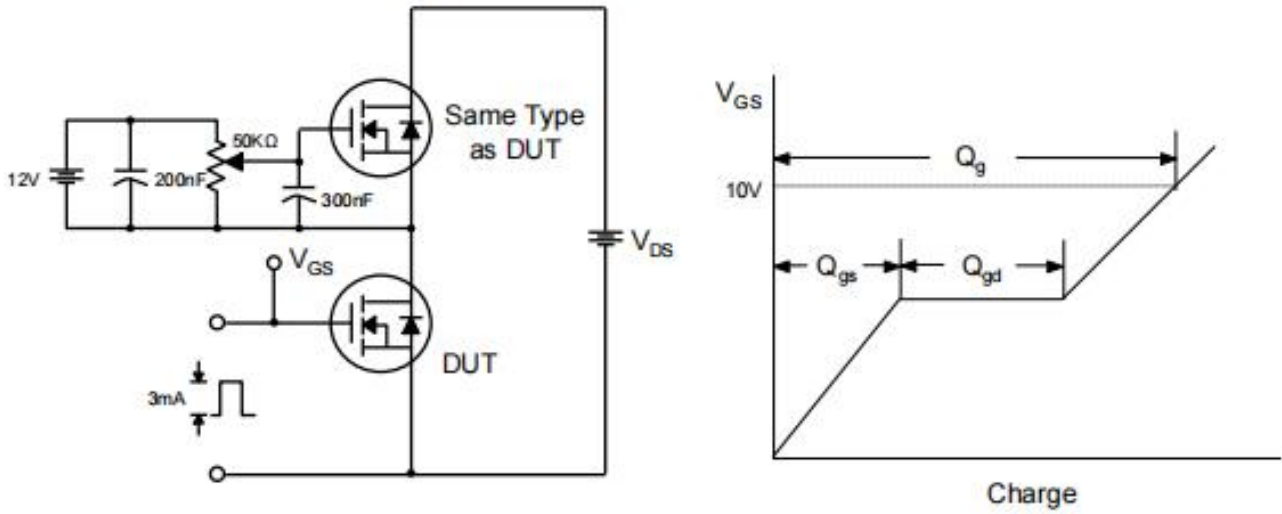


Fig 13. Resistive Switching Test Circuit & Waveforms

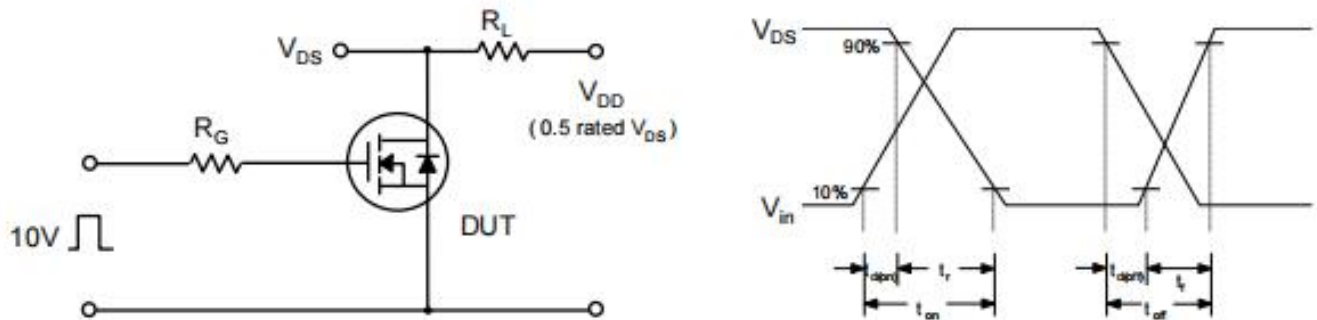
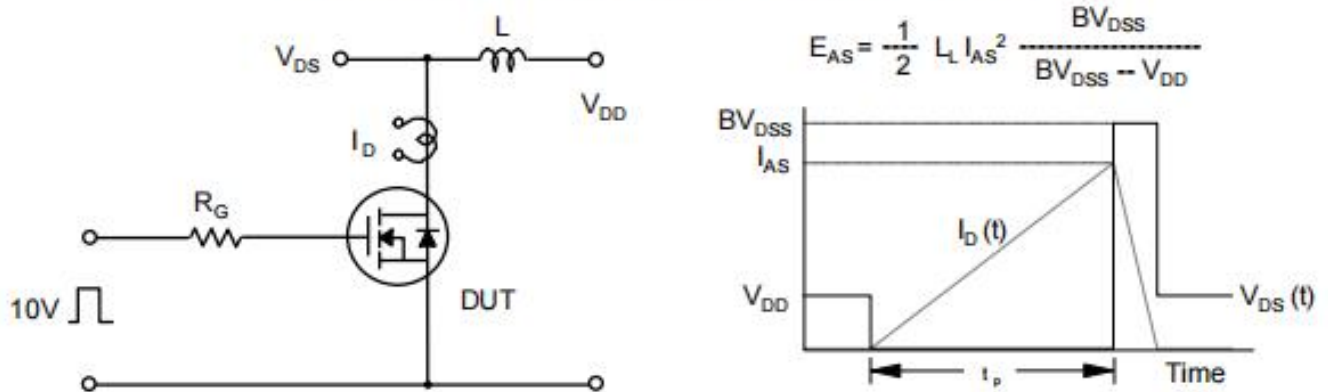
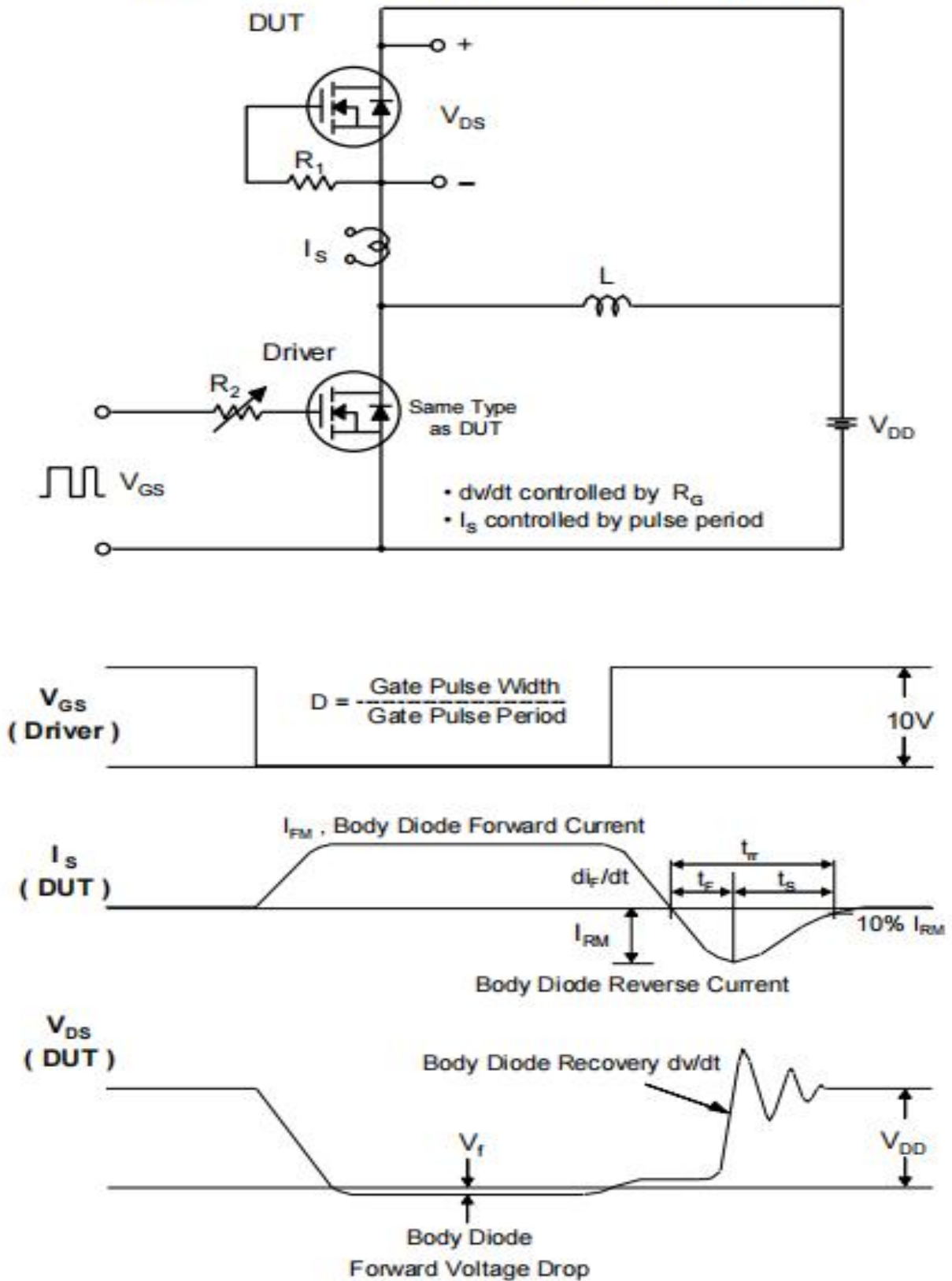


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

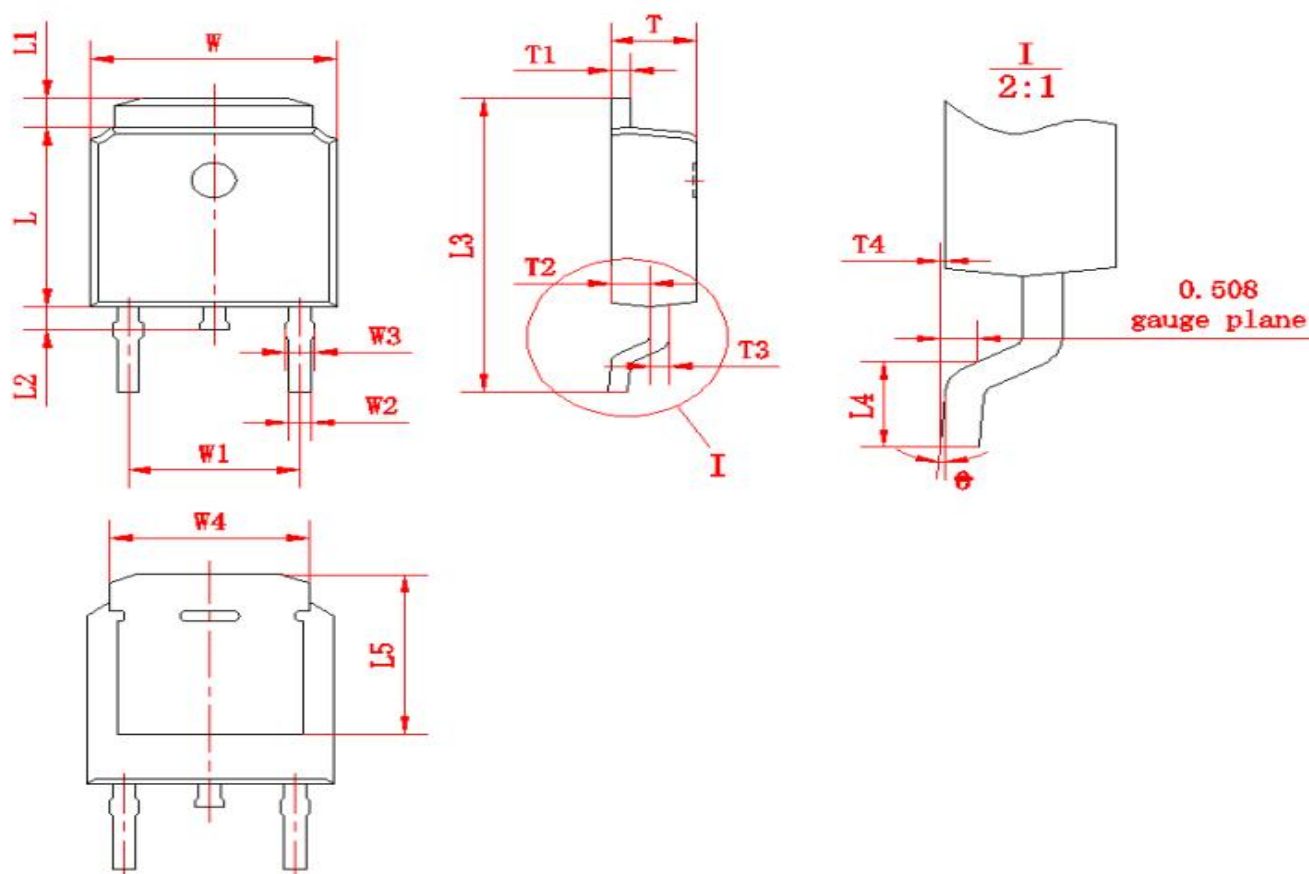


Test Circuits and Waveforms

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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