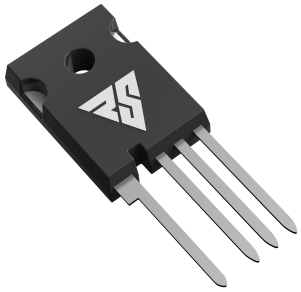
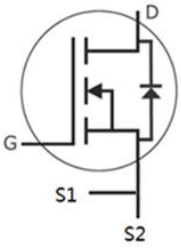
VDS	RDS(on)	ID@25℃
1200V	40mΩ	67A





S1: Driver Source
S2: Power Source

Applications:

- Renewable Energy
- Switch Mode Power Supplies
- EV Battery Chargers
- High voltage DC-DC converters

Features:

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive

Benefits:

- HigherSystemEfficiency
- ReducedCoolingRequirements
- IncreasedPowerDensity
- IncreasedSystemSwitchingFrequency

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSM12H040Z	TO-247-4	RSM12H040Z	Tube	30 PCS

Maximum Ratings（TJ= 25℃ unless otherwise specified）

Symbol	Parameter	Value	Unit	Test Conditions	Note
VDSmax	Drain - Source Voltage	1200	V	VGS=0V,ID =100μA	
VGSmax	Gate - Source Voltage	-10/+23	V	Absolute maximum values	
VGSop	Gate - Source Voltage	-5/+18	V	Recommended operational values	
ID	Continuous Drain Current	67 47	A	VGS=18V,TC =25℃ VGS=18V,TC =100℃	
ID(pulse)	Pulsed Drain Current	201	A	Pulse width tp limited by TJmax	
PD	Power Dissipation	375	W	TC =25℃,Tj =175℃	
TL	Solder Temperature,1.6mm from case for 10s	260	℃		
TJ, Tstg	Operating Junction and StorageTemperature	-55 to + 175	℃		
Md	Mounting Torque, (M3 or 6-32 screw)	1 8.8	Nm lbf-in		

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Electrical Characteristics （TJ= 25℃ unless otherwise specified）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V(BR) DSS	Drain-Source Breakdown Voltage	1200			V	VGS=0V,ID =100μA
VGS(th)	Gate Threshold Voltage	2.0	2.8	4.0	V	VGS= VDS, ID=9.2mA
			2.0		V	VGS= VDS, ID=9.2mA,TJ=175℃
IDSS	Zero Gate Voltage Drain Current		1	100	μA	VDS= 1200V, VGS=0V
IGSS	Gate-Source Leakage Current		10	100	nA	VGS=23V, VDS= 0V
			-10	-100	nA	VGS=-10V, VDS= 0V
RDS(on)	Drain-Source on-state Resistance		40	52	mΩ	VGS=18V, ID =33.3A
			60			VGS=18V, ID =33.3A, TJ=175℃
Gfs	Forward transconductance		21		S	VDS=20V,ID=33.3A
			20.5			VDS=20V,ID=33.3A,TJ=175℃
Ciss	Input Capacitance		2320		pF	VGS=0V, VDS=1000 V f=1MHz，VAC=25 mV
Coss	Output Capacitance		89			
Crss	Reverse Transfer Capacitance		8			
Eoss	Stored Energy inOutputCapacitance		45		μJ	
EON	Turn-On Switching Energy		600			VDS =800V, VGS =-5/18V ID = 30A,RG(ext) = 2.5Ω L= 100μH
EOFF	Turn-Off Energy		60			
td(on)	Turn-On Delay Time		14		ns	VDS =800V, VGS =-5/18V ID = 33.3A,RG(ext) = 2.5Ω RL=24Ω
tr	Rise Time		19			
td(off)	Turn-Off Delay Time		28			
tf	Fall Time		7.4			
RG	Internal Gate Resistance		3.1		Ω	f=1 MHz, VAC=25MV
Qgs	Gate to Source Charge		32		nC	VDS=800V VGS=-5/18V ID =33.3A
Qgd	Gate to Drain Charge		20			
Qg	Total Gate Charge		108			

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Reverse Diode Characteristics (TJ= 25℃ unless otherwise specified)

Symbol	Parameter	Typ.	Max	Unit	Test Conditions
VSD	Diode Forward Voltage	4.2		V	VGS=-5V, ISD = 16.5A, TJ = 25℃
		3.6		V	VGS=-5V, ISD= 16.5A, TJ= 175℃
IS	Continuous Diode Forward Current		67	A	TC= 25℃
trr	Reverse Recovery time	23		ns	VR = 800V ISD=33.3A
Qrr	Reverse Recovery Charge	279		nC	
Irrm	Peak Reverse Recovery Current	16		A	

Thermal Characteristics (TJ= 25℃ unless otherwise specified)

Symbol	Parameter	Typ.	Max	Unit	Test Conditions
RθJC	Thermal Resistance from Junction to Case	0.40		℃/W	
RθJA	Thermal Resistance From Junction to Ambient		40		

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Typical Feature Curve

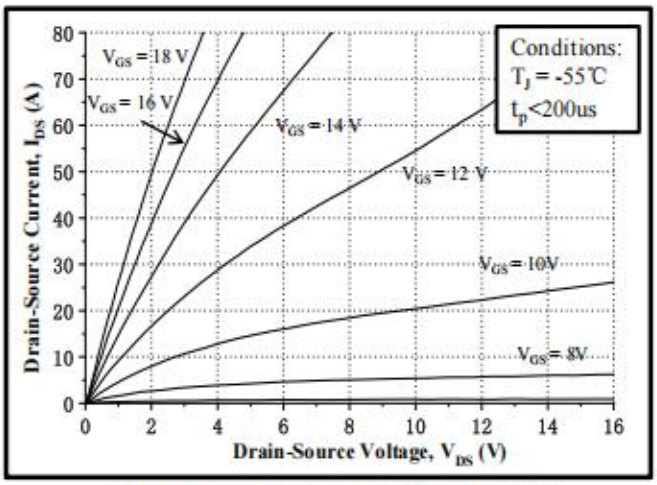

Figure 1. Output Characteristics T_J = -55℃

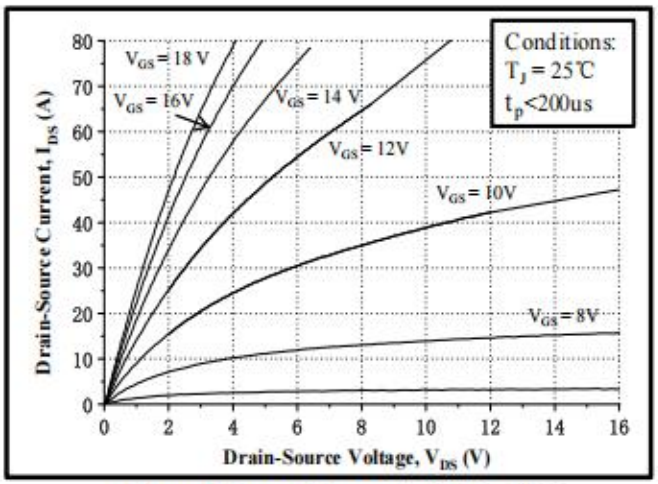

Figure 2. Output Characteristics T_J= 25℃

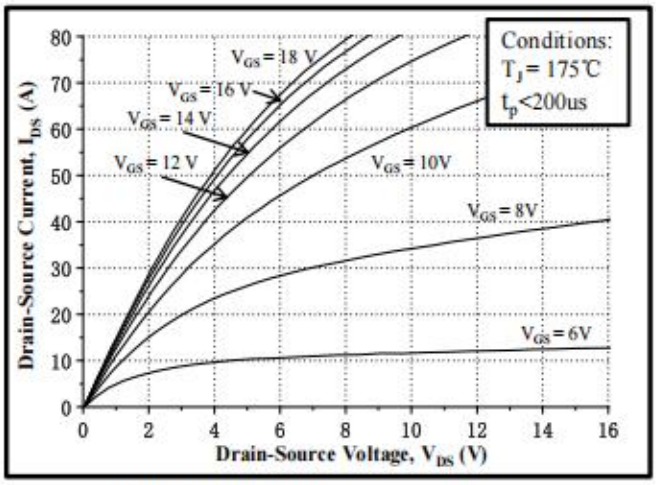

Figure 3. Output Characteristics T_J = 175℃

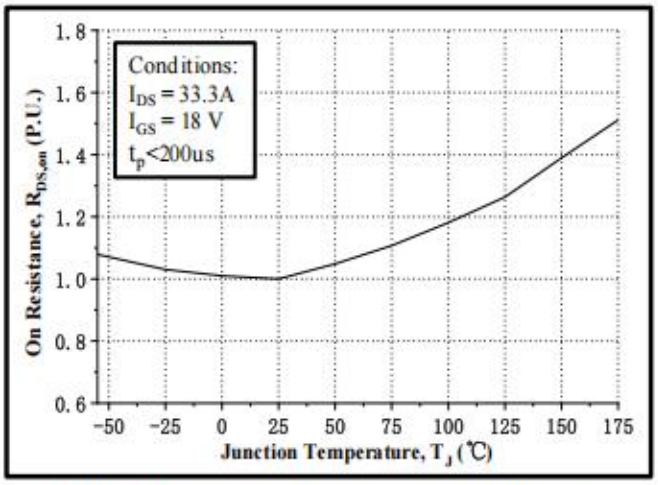

Figure 4. Normalized On-Resistance vs. Temperature

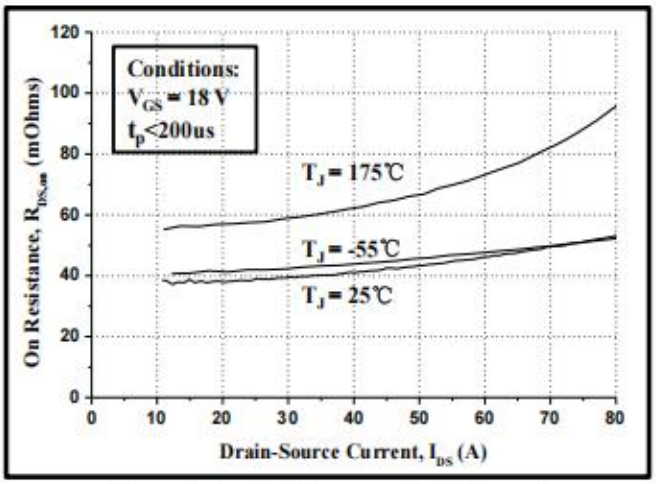

Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

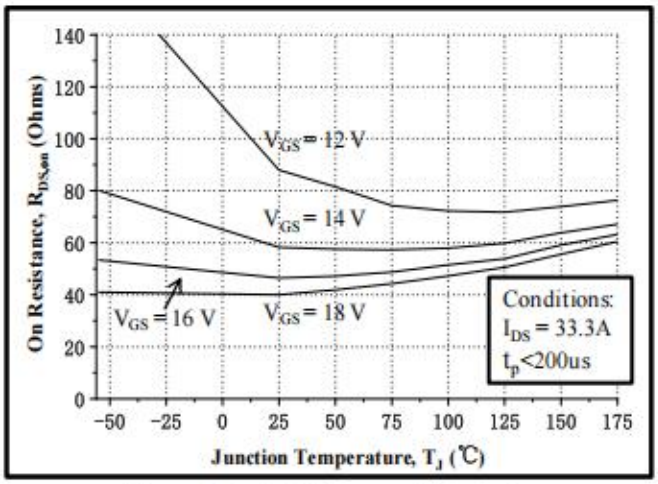

Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

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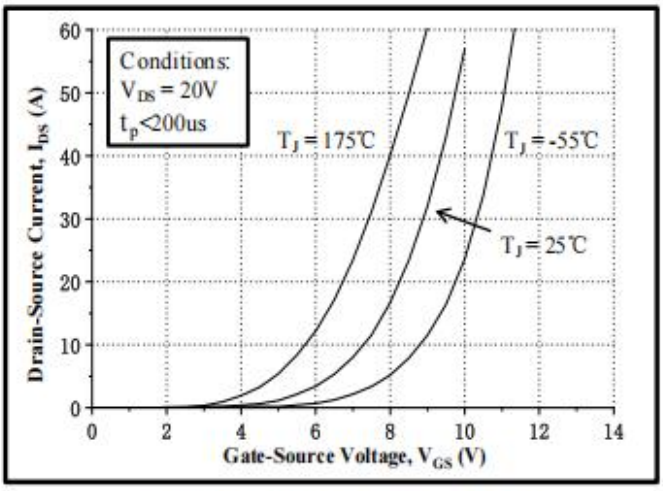

Figure 7. Transfer Characteristic for Various Junction Temperatures

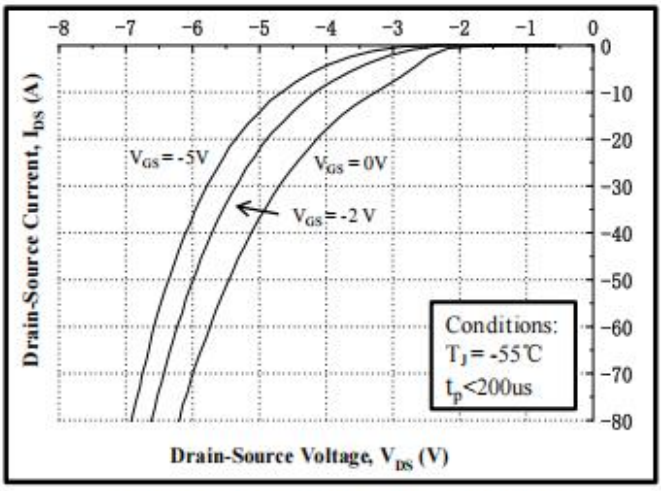

Figure 8. Body Diode Characteristic at -55℃

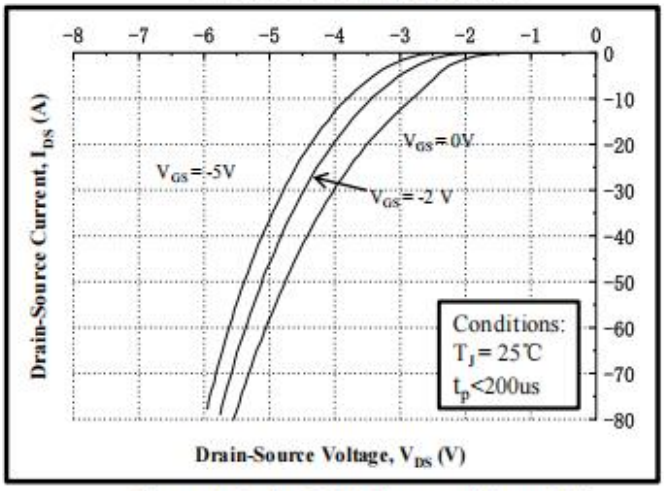

Figure 9. Body Diode Characteristic at 25℃

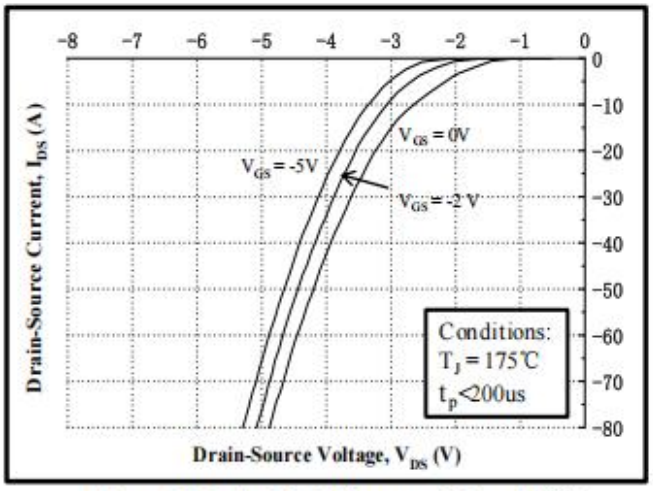

Figure 10. Body Diode Characteristic at 175℃

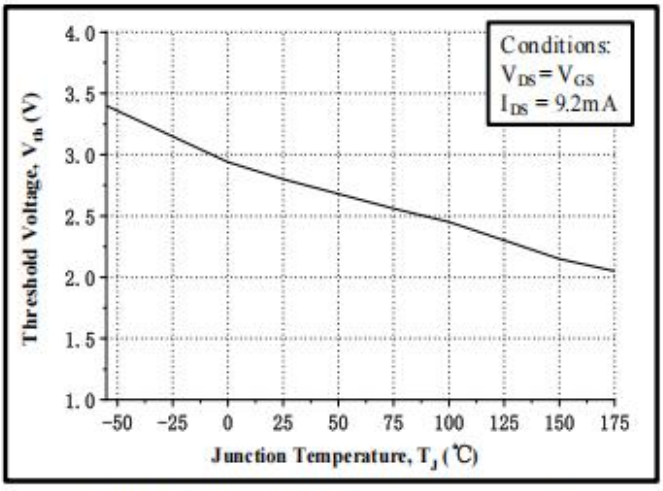

Figure 11. Threshold Voltage vs. Temperature

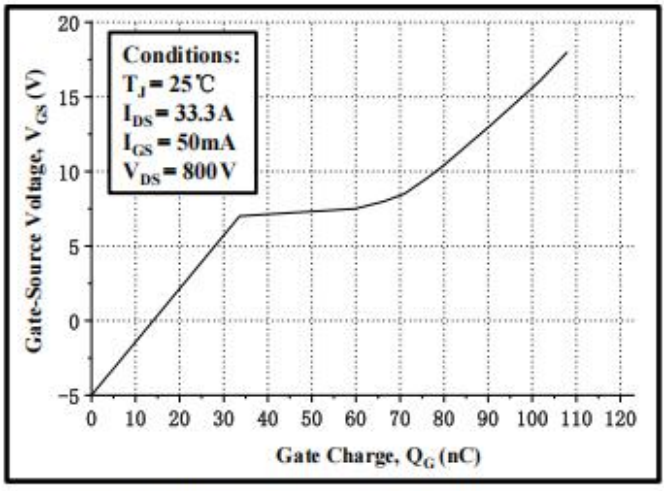

Figure 12. Gate Charge Characteristics

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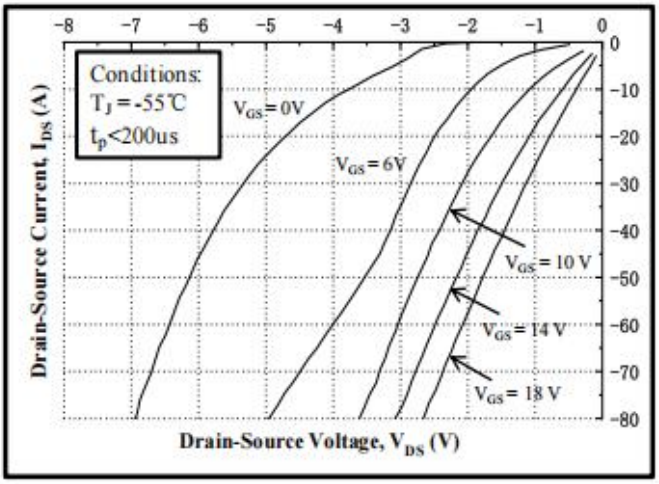

Figure 13. 3rd Quadrant Characteristic at -55℃

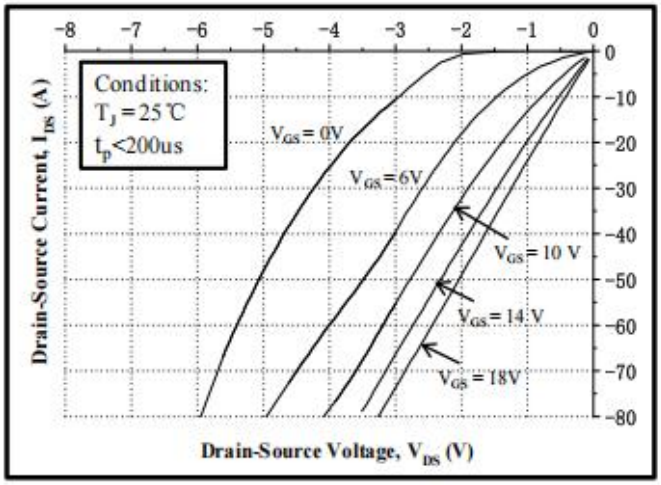

Figure 14. 3rd Quadrant Characteristic at 25℃

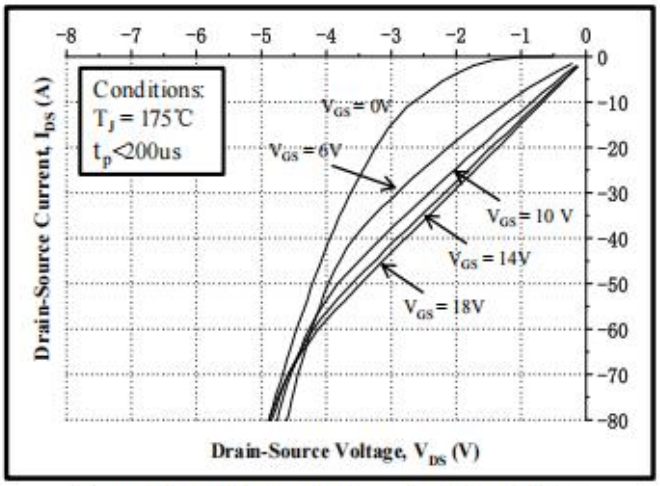

Figure 15. 3rd Quadrant Characteristic at 175 ℃

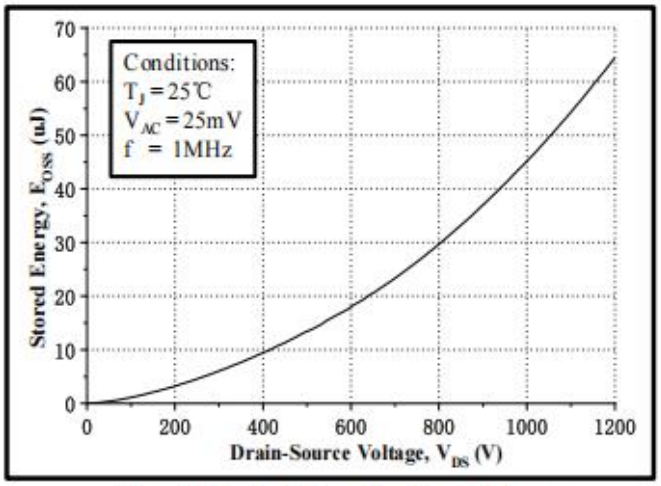

Figure16. Output Capacitor Stored Energy

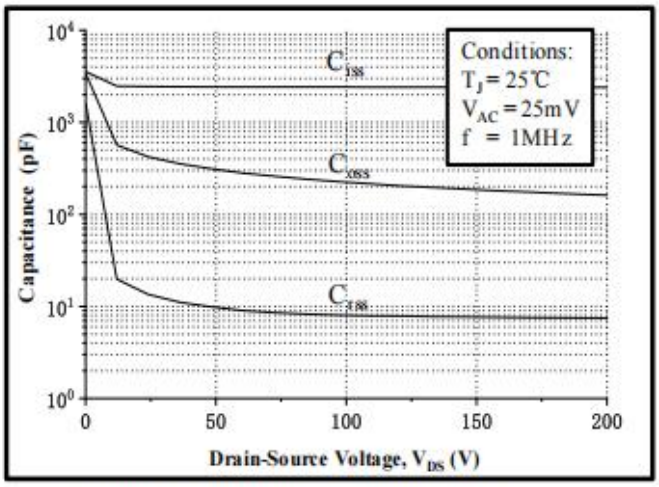

Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

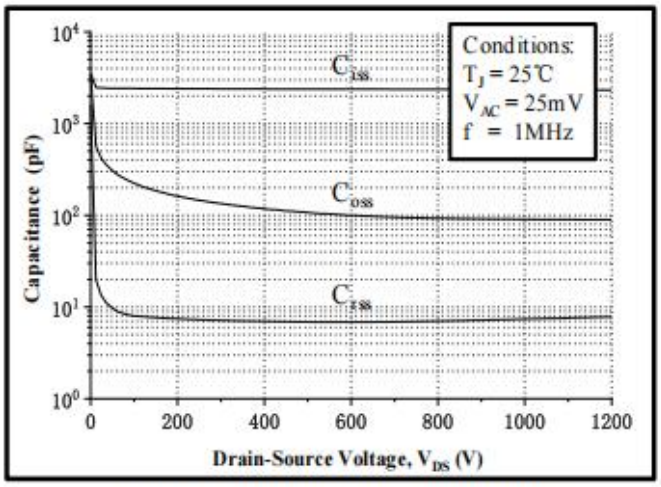

Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

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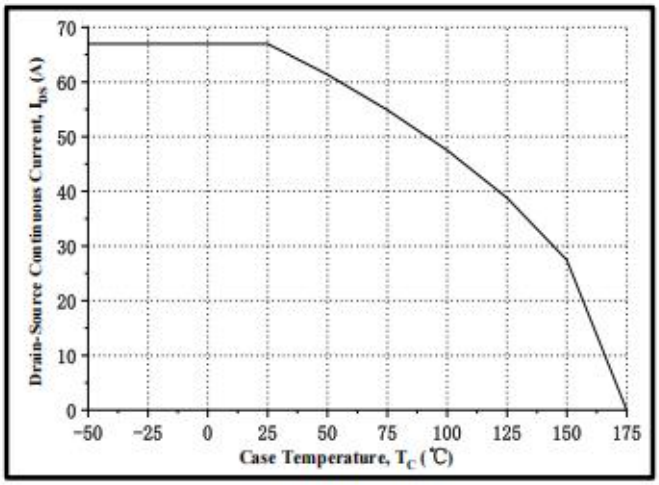

Figure 19. Continuous Drain Current Derating vs. Case Temperature

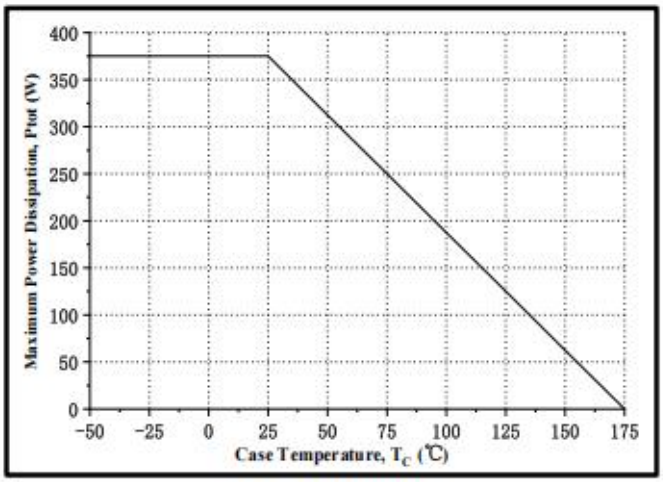

Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

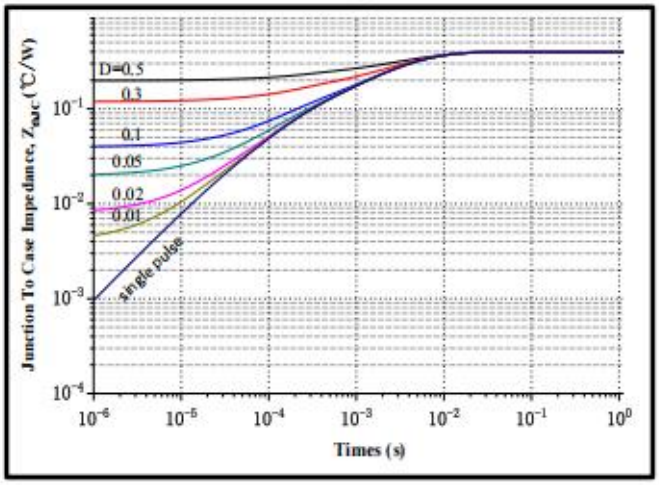

Figure 21. Transient Thermal Impedance (Junction - Case)

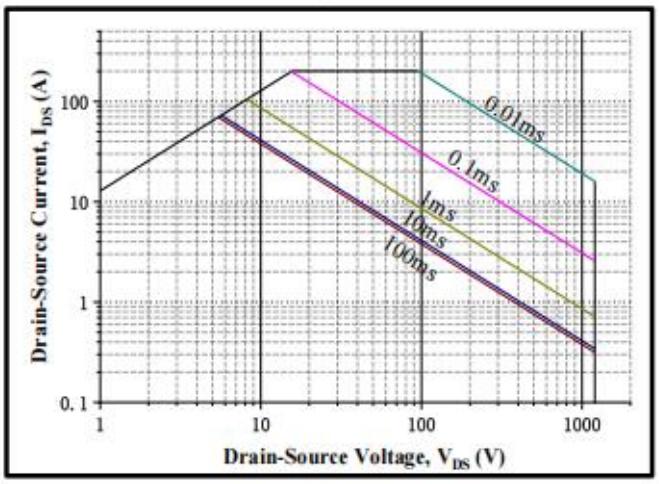

Figure22. Safe Operating Area

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Test Circuit Schematic

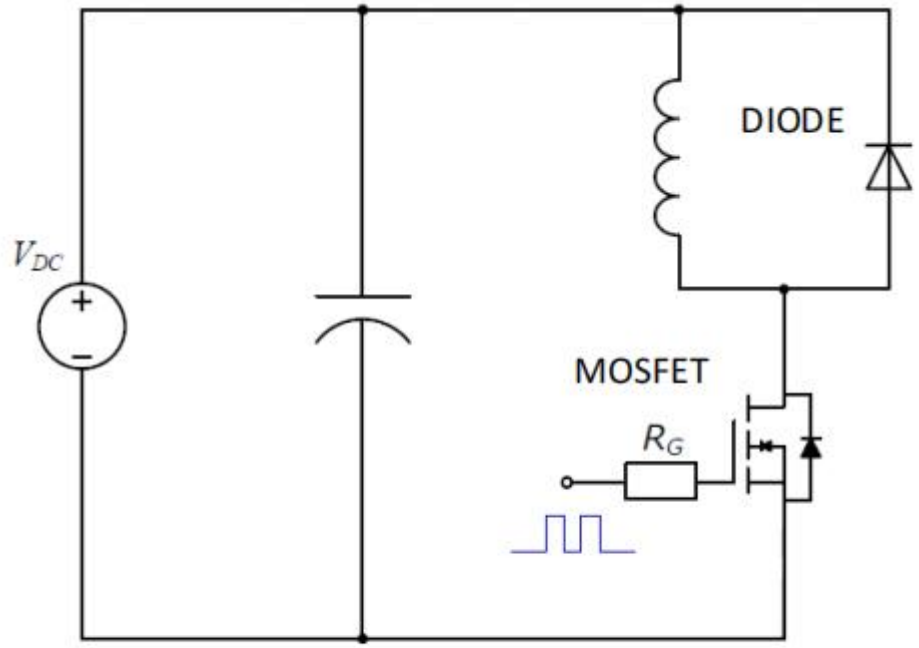

Figure 23. Clamped Inductive Switching Waveform Test Circuit

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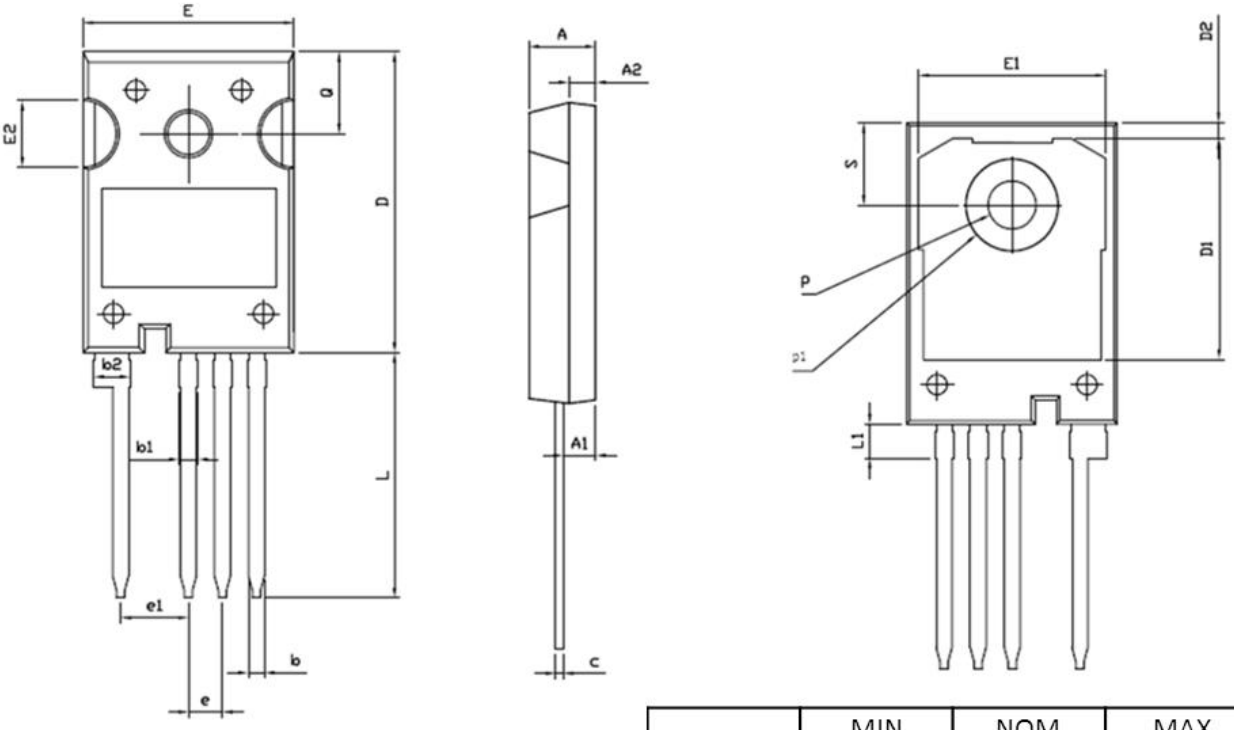
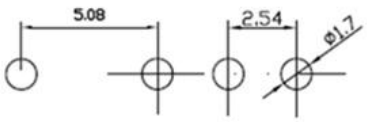
Package outline drawing(TO-247-4 Unit: mm)



RECOMMENDED LAND PATTERN



UNIT: mm

	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.25	2.40	2.55
A2	1.85	2.00	2.15
b	1.05	1.20	1.35
b1	1.00	1.30	1.60
b2	2.35	2.65	2.95
c	0.50	0.60	0.70
D	22.29	22.54	22.79
D1	16.00	16.50	17.00
D2	0.97	1.17	1.37
e	2.34	2.54	2.74
e1	4.88	5.08	5.28
E	15.60	15.80	16.00
E1	13.50	14.00	14.50
E2	4.80	5.00	5.20
L	18.08	18.38	18.68
L1	2.38	2.58	2.78
p	3.50	3.60	3.70
p1	6.60	7.10	7.60
Q	6.00	6.15	6.30
S	6.00	6.15	6.30

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c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.

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