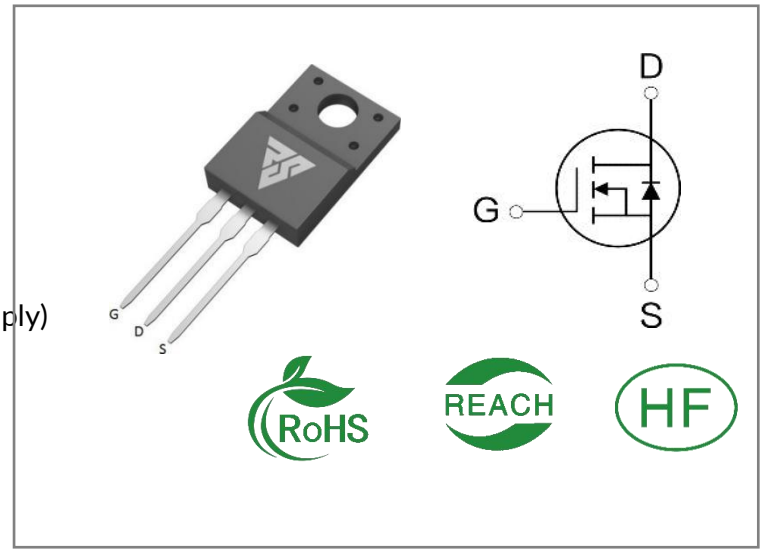
ID	R_{DS}(ON)(Typ)	VDSS
40A	78mΩ	500V



Applications:

- TV and PC Power
- Adopter and Lighting
- Telecom and UPS(Uninterruptible Power Supply)

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability
- VDS @ Tj max 700V

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS50R090F	T0-220F	RS50R090F	Tube	50 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS50R090F	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current TC=25℃	40	A
ID	Continuous Drain Current TC=100℃	24	
IDM	Pulsed Drain Current	63	
PD	Power Dissipation	35	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=10mH,VDS= 50V, RG=25Ω,TJ=25℃	550	mJ
dv/dt	MOSFET dv/dt ruggedness VDS = 0...400V	50	V/ns
dv/dt	Reverse diode dv/dt VDS = 0...400V Tj = 25℃, ISD≤ID	15	
TL TPKG	Maximum Temperature for Soldering	300	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS50R090F	Units	Test Conditions
RθJC	Junction-to-Case	3.7	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to- Ambient	80		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500	--	--	V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=500V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	78	90	mΩ	VGS=10V ID=18A
VGS(TH)	Gate Threshold Voltage	2	--	4	V	VGS=VDS ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	35	--	nS	VDS=400V ID=24A RG=2.5Ω
trise	Rise Time	--	34	--		
td(OFF)	Turn- OFF Delay Time	--	50	--		
tfall	Fall Time	--	4.8	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	2110	--	pF	VGS=0V VDS=100V f=1.0MHz
Coss	Output Capacitance	--	82	--		
Crss	Reverse Transfer Capacitance	--	0.7	--		
Qg	Total Gate Charge	--	51	--	nC	VDS=480V ID=24A VGS=10V
Qgs	Gate- to- Source Charge	--	11	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	22	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	40	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	120	A	
VSD	Diode Forward Voltage	--	--	1.0	V	IS=40A VGS=0V
trr	Reverse Recovery Time	--	368	--	nS	VR=300V IS=24A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	3.5	--	μC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.

Typical Feature Curve

Figure 1. Typical Output Characteristics

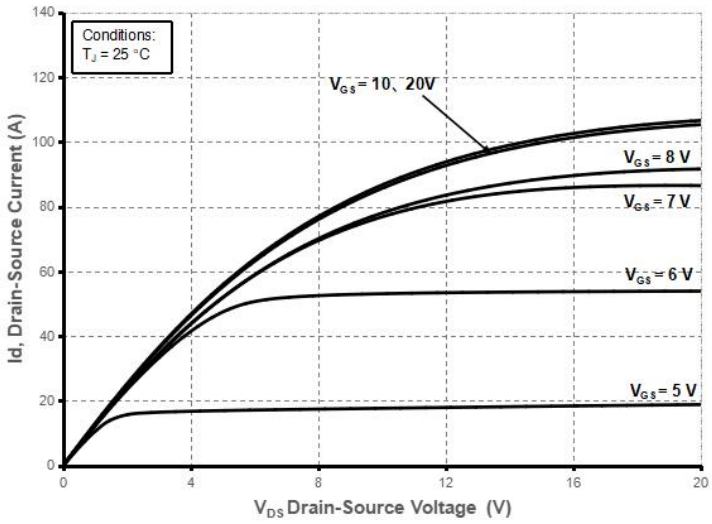


Figure 2. Typical Transfer Characteristics

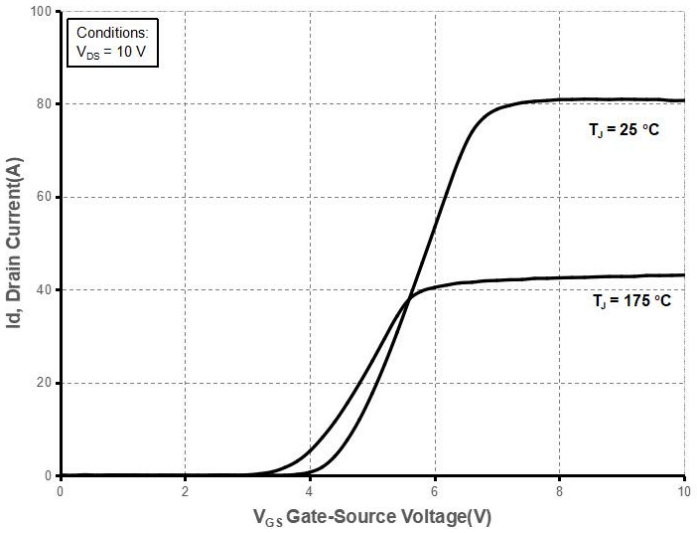


Figure 3. On-Resistance versus Drain Current

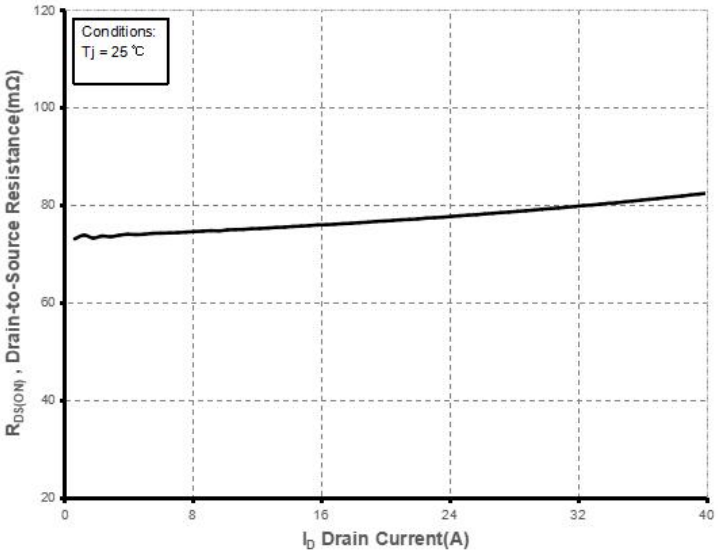


Fig 4. Diode forward voltage versus Current

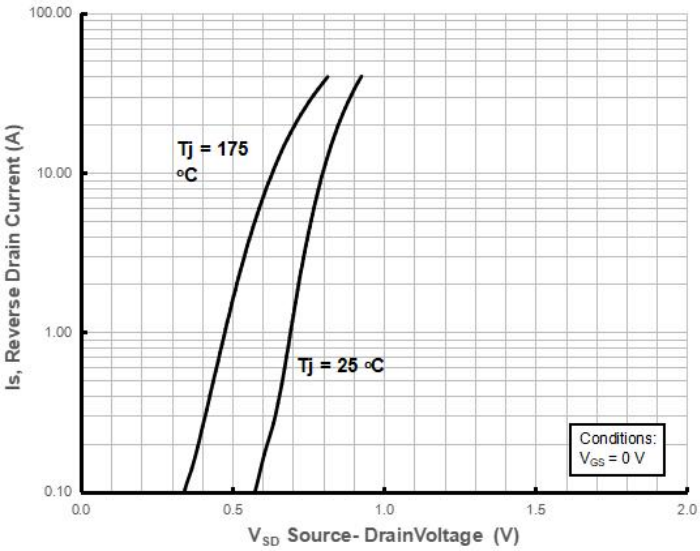


Figure 5. Typical Capacitance versus VDS

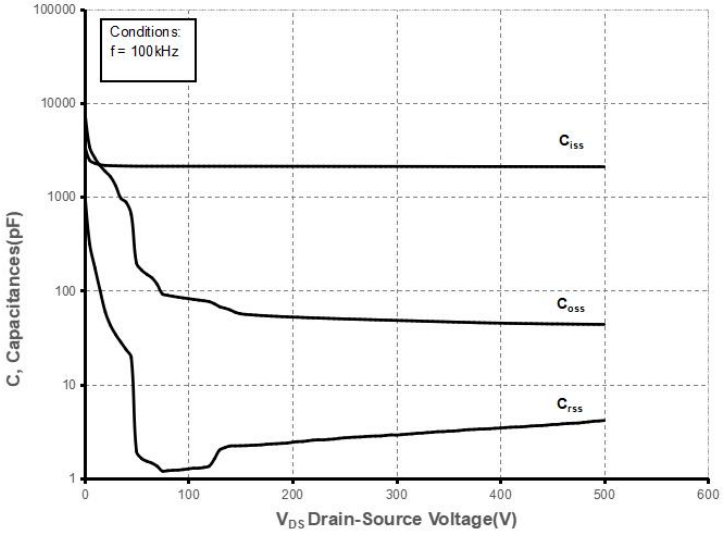


Figure 6. Typical Gate Charge versus VGS

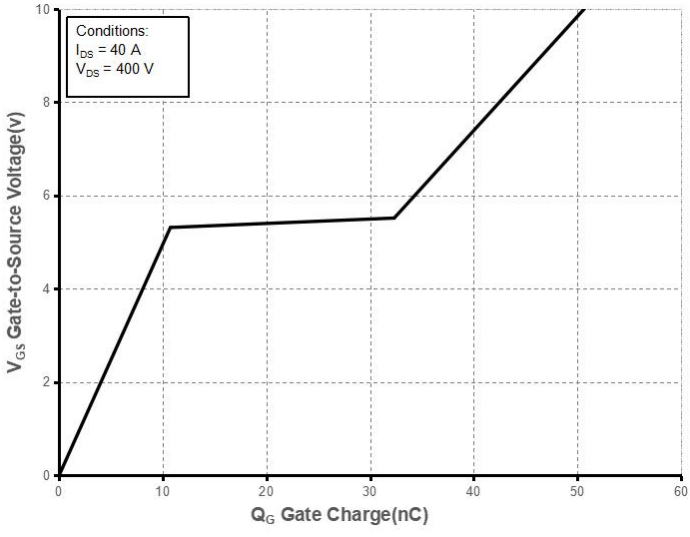


Figure 7. BVDSS Variation with Temperature

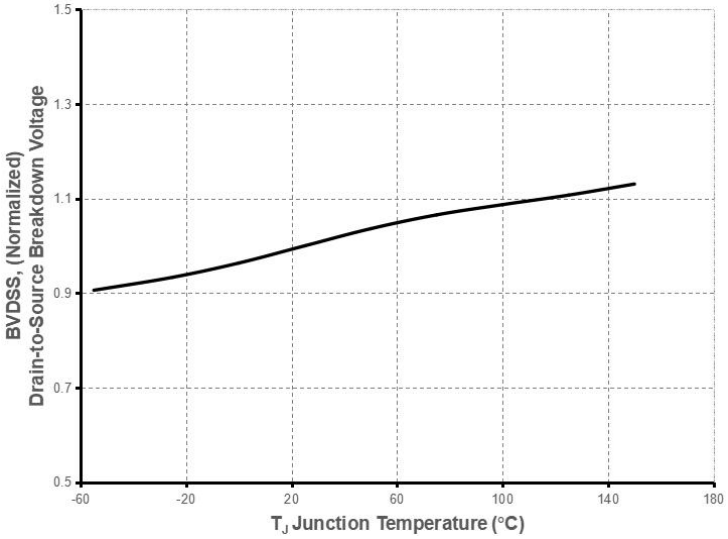


Figure 8. On-Resistance Variation with Temperature

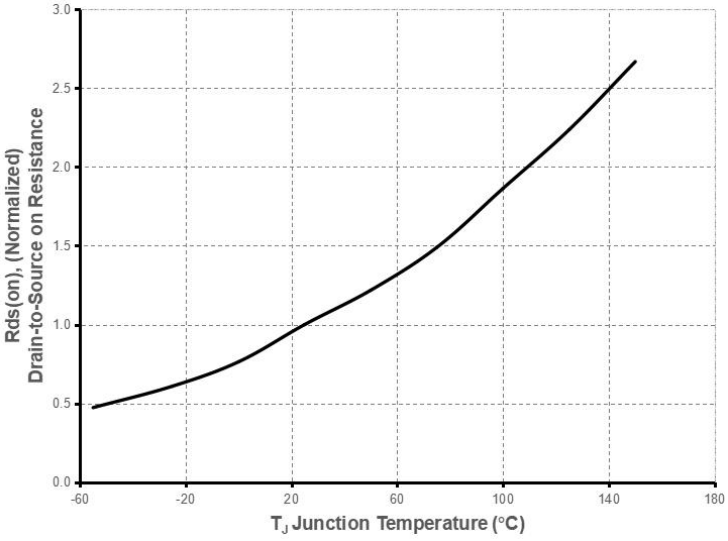


Figure 9. Maximum Safe Operating Area

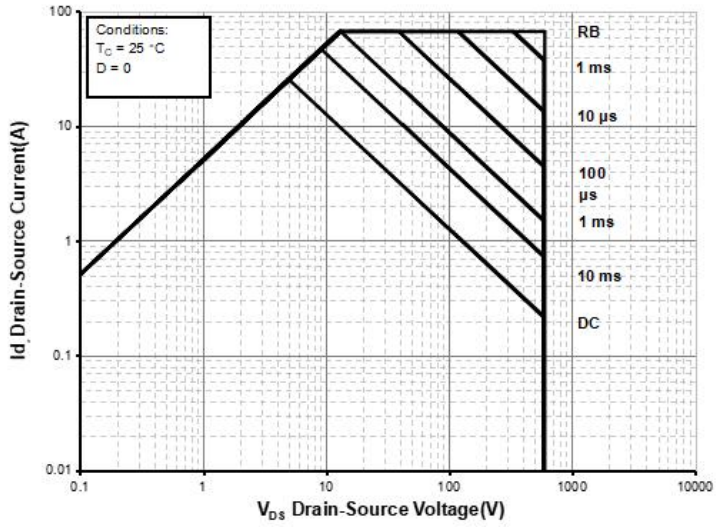
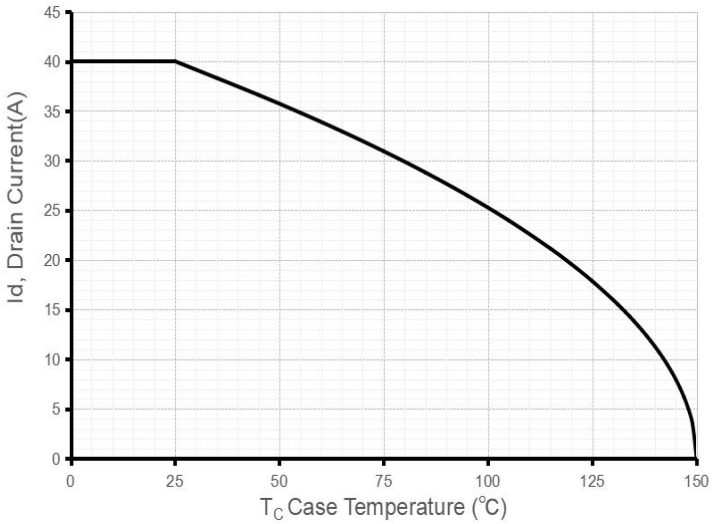


Figure 10. Maximum Continuous Drain versus Case Temperature



Test Circuits and Waveforms

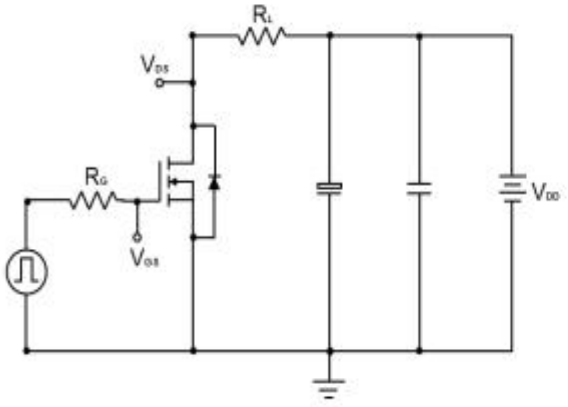


Fig. 12 Test circuit for resistive load switching times

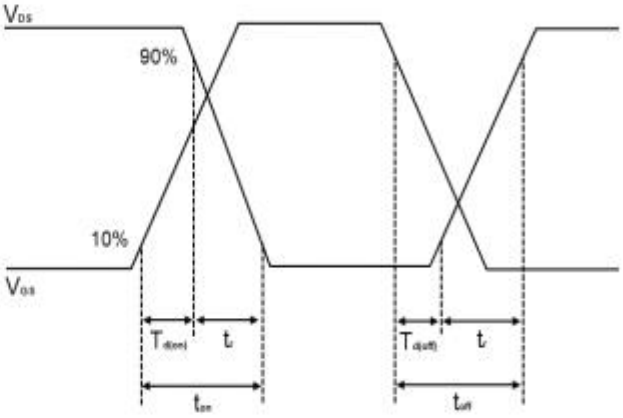


Fig. 13 Switching times waveform

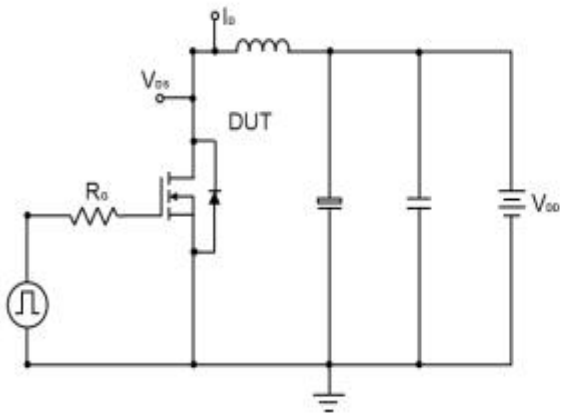


Fig. 14 Test circuit for unclamped inductive load

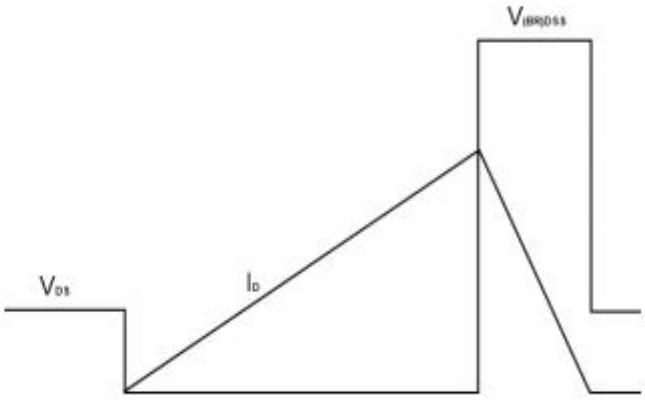


Fig. 15 Unclamped inductive waveform

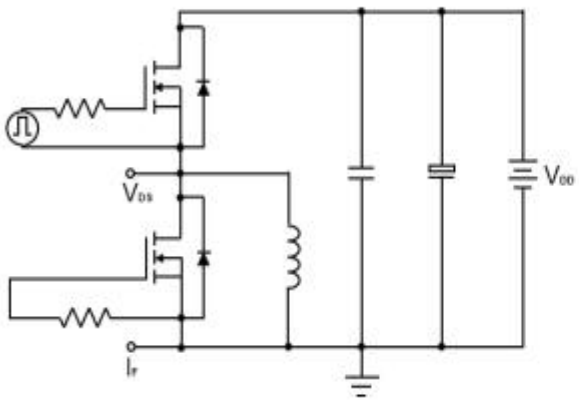


Fig. 16 Test circuit for diode characteristics

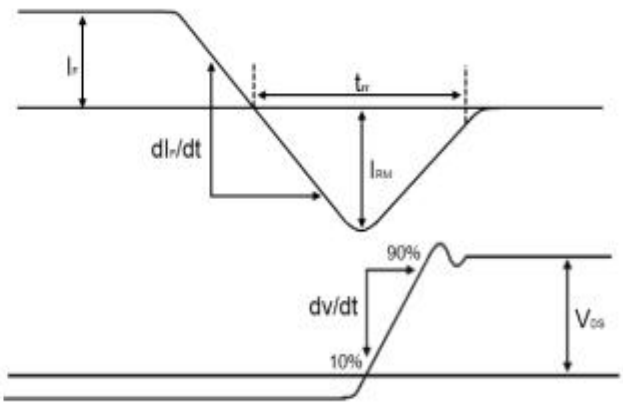
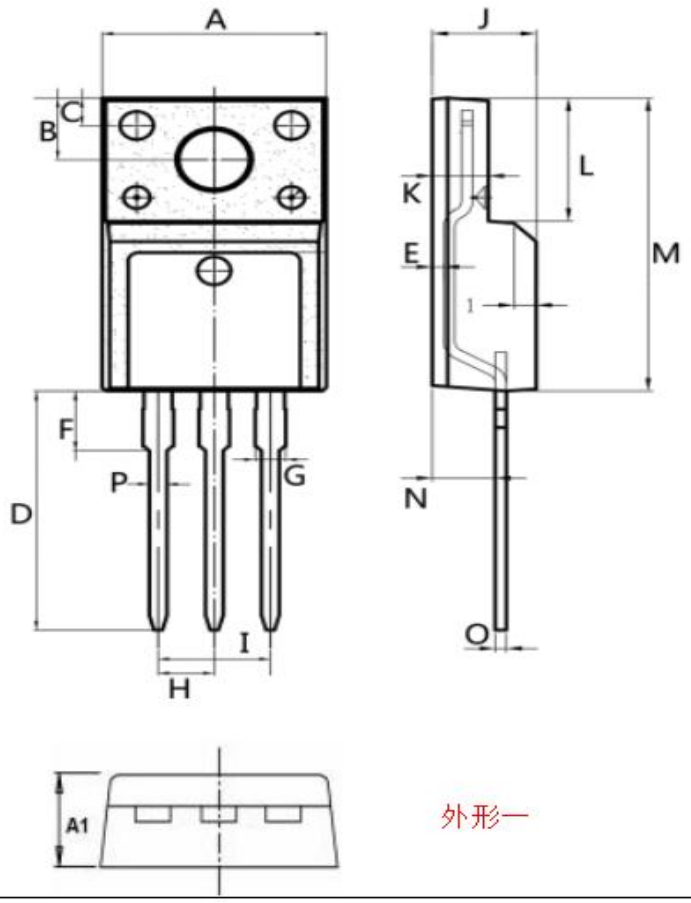


Fig. 17 Diode recovery waveform

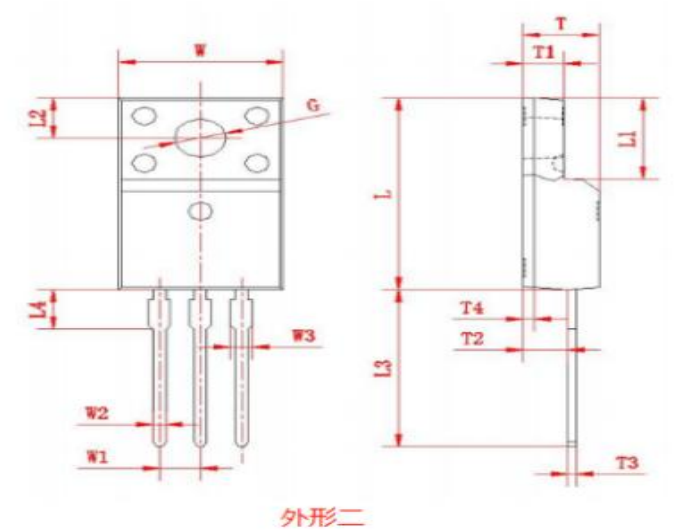
Package outline drawing(TO-220F Unit: mm)



外形一

Dim.	Min.	Max.
A	9.95	10.36
A1	4.5	5.0
B	2.95	3.25
C	1.25	1.45
D	12.60	13.60
E	0.40	0.60
F	2.8	3.5
G	1.30	1.45
H	(2.54)	
I	(5.08)	
J	4.60	4.75
K	2.45	2.65
L	6.5	6.8
M	15.4	16.0
N	2.25	3.05
O	0.45	0.55
P	0.70	0.90

All Dimensions in millimeter



外形二

Dim.	Min.	Max.
W	9.95	10.36
W1	(2.54)	
W2	0.70	0.90
W3	1.25	1.47
L	15.67	16.07
L1	6.48	6.88
L2	3.2	3.4
L3	12.6	13.6
L4	(3.23)	
T	4.50	4.90
T1	2.34	2.74
T2	2.25	2.95
T3	0.45	0.60
T4	(0.70)	
G	3.08	3.28

All Dimensions in millimeter

Disclaimers:

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights,nor the rights of others.Reproduction of inform- ation in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as cri- tical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.

As used herein:

1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.