

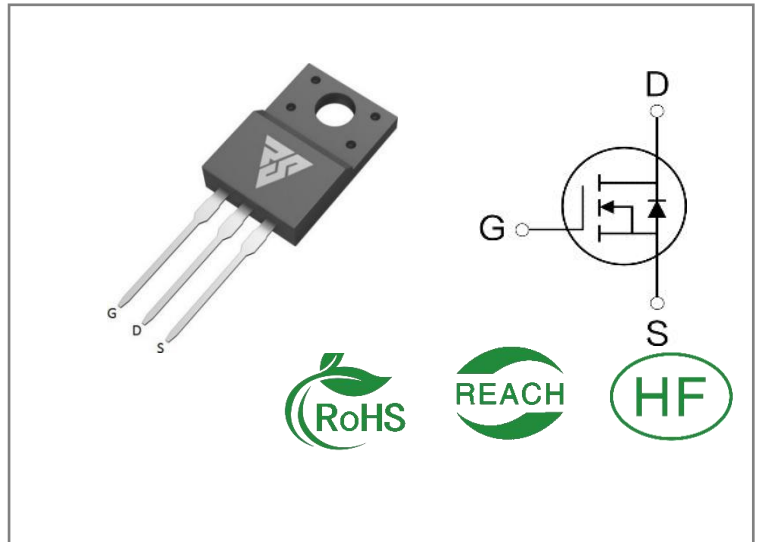
ID	$R_{DS(ON)}$ (Typ)	VDSS
20A	160mΩ	600V

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC-DC Switching Power Supply

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability



Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS60R190BF	T0-220F	RS60R190BF	Tube	50 PCS

Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	RS60R190BF	Units
VDSS	Drain-to-Source Voltage	600	V
ID	Continuous Drain Current $T_C=25^\circ\text{C}$	20	A
ID	Continuous Drain Current $T_C=100^\circ\text{C}$	13	
IDM	Pulsed Drain Current (Note*1)	60	
PD	Power Dissipation	34	W
VGS	Gate- to- Source Voltage	± 30	V
EAS	Single Pulse Avalanche Energy $L=10\text{mH}, V_{DS}=50\text{V}, R_G=25\Omega, T_C=25^\circ\text{C}$	310	mJ
dv/dt	MOSFET dv/ dt ruggedness $V_{DS}=0\ldots 400\text{V}$	50	V/ns
dv/dt	Reverse diode dv/dt $V_{DS}=0\ldots 400\text{V}, T_j=25^\circ\text{C}, I_{SD}\leq I_D$	15	V/ns
TL TPKG	Maximum Temperature for Soldering	300	$^\circ\text{C}$
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS60R190BF	Units	Test Conditions
R θ JC	Junction-to-Case	3.7	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\text{C}$
R θ JA	Junction-to- Ambient	80		1 cubic foot chamber, free air.

OFF Characteristics TJ= 25 $^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	600	--	--	V	VGS=0V ID=250 μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=600V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics TJ=25 $^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	160	185	m Ω	VGS=10V ID=10A
VGS(TH)	Gate Threshold Voltage	2.0	--	4.1	V	VGS=VDS ID=250 μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	23	--	nS	VDS=300V ID=20A RG=25 Ω
trise	Rise Time	--	35	--		
td(OFF)	Turn- OFF Delay Time	--	113	--		
tfall	Fall Time	--	28	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1490	--	pF	VGS=0V VDS=50V f=1.0MHz
Coss	Output Capacitance	--	101	--		
Crss	Reverse Transfer Capacitance	--	2.3	--		
Qg	Total Gate Charge	--	36	--	nC	VDS=520V ID=20A VGS=10V
Qgs	Gate- to- Source Charge	--	7.2	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	16	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	20	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	60	A	
VSD	Diode Forward Voltage	--	--	1.0	V	IS=20A VGS=0V
trr	Reverse Recovery Time	--	347	--	nS	VR=100V IS=20A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	5	--	μC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

Typical Feature Curve

Figure1. Output Characteristics

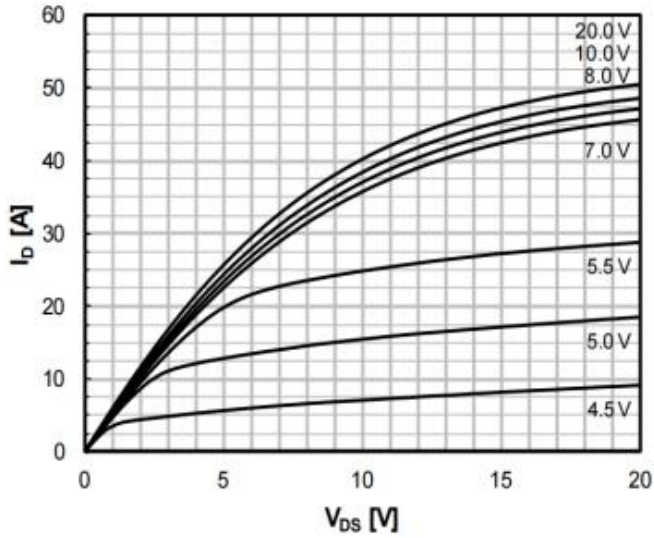


Figure2. Transfer Characteristics

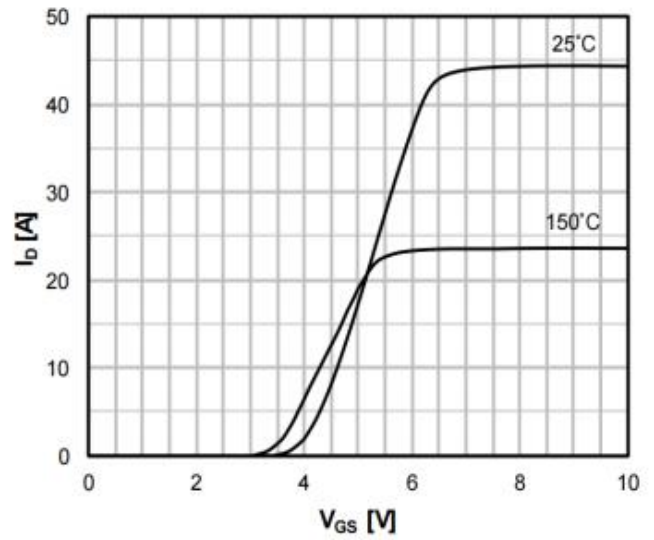


Figure 3. On-Resistance VS.Drain Current

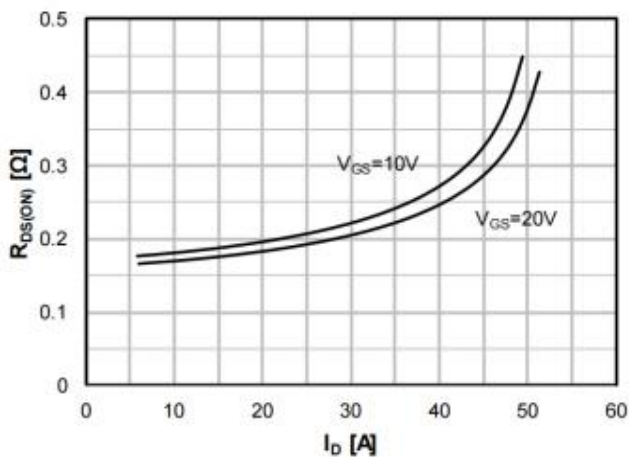


Figure 4. Capacitance

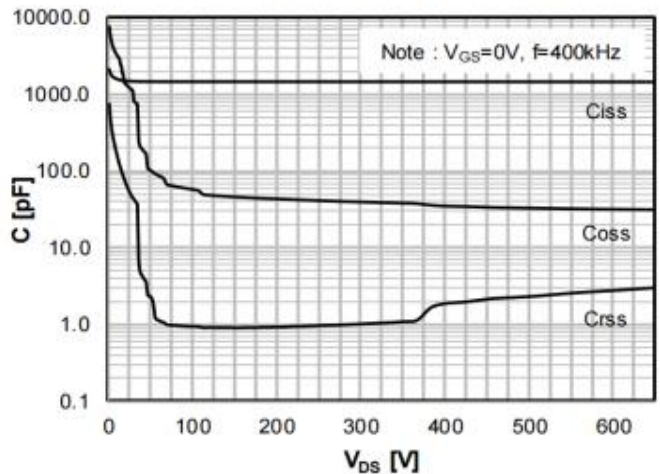


Figure 5. Gate Charge

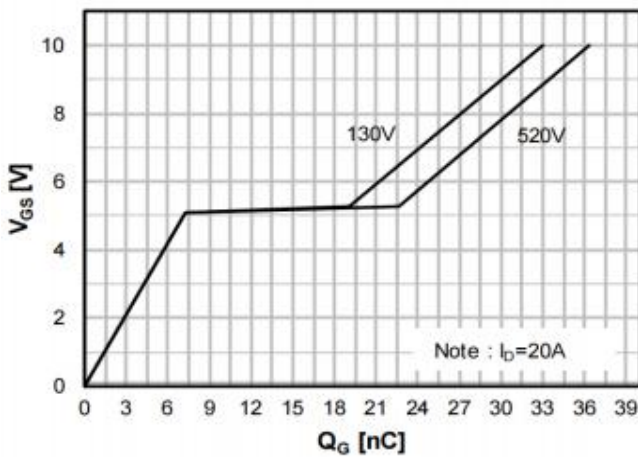


Figure 6. Body Diode Forward Voltage

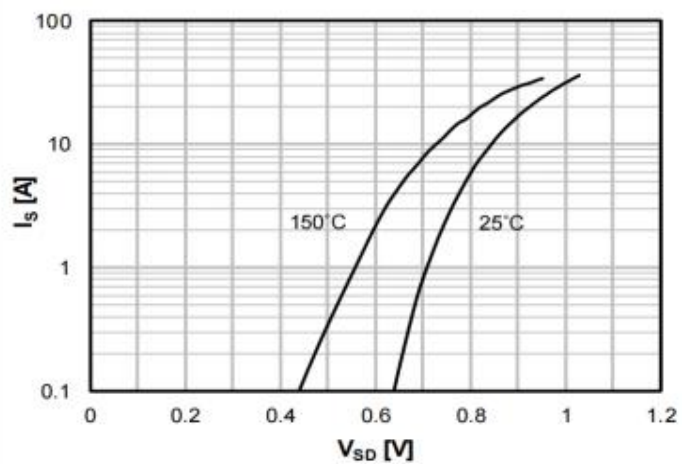


Figure 7. On-Resistance vs. Junction Temperature

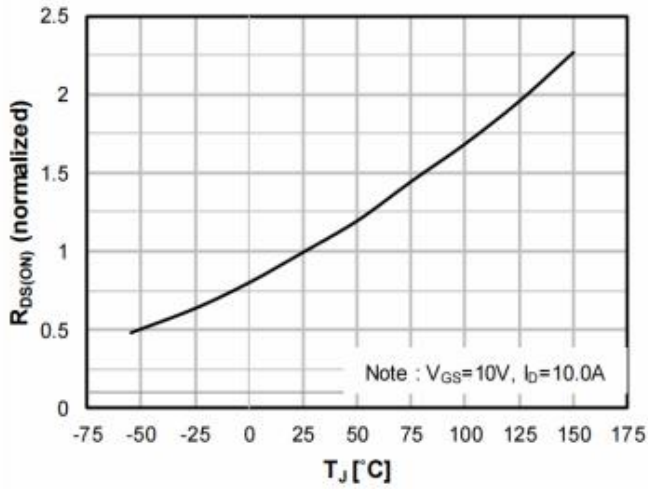


Figure 8. Breakdown Voltage vs. Junction Temperature

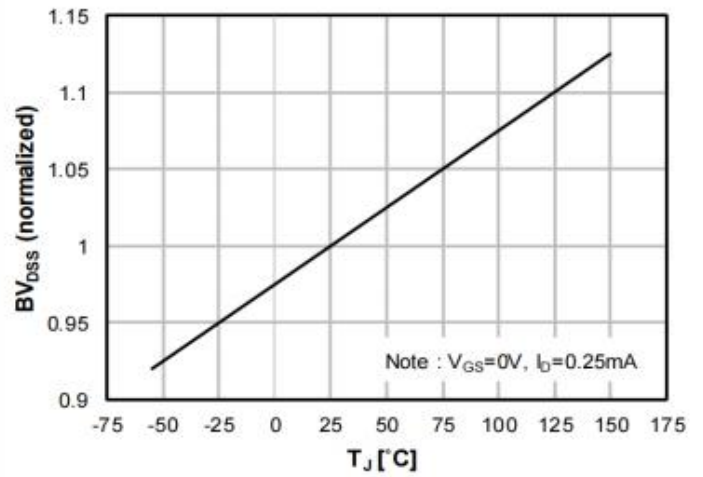


Figure 9. Safe operation area

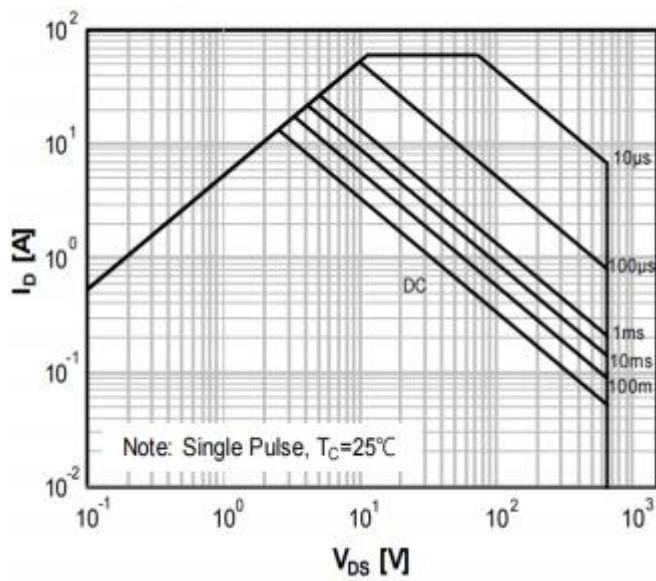
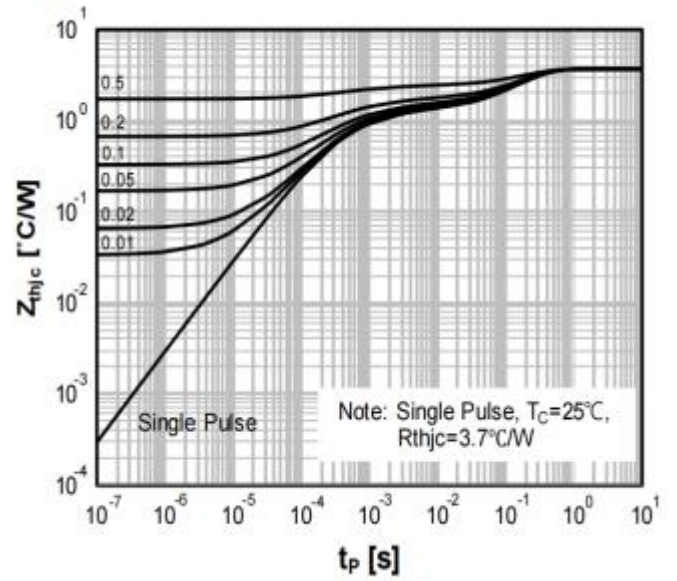


Figure 10. Transient Thermal Impedance



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

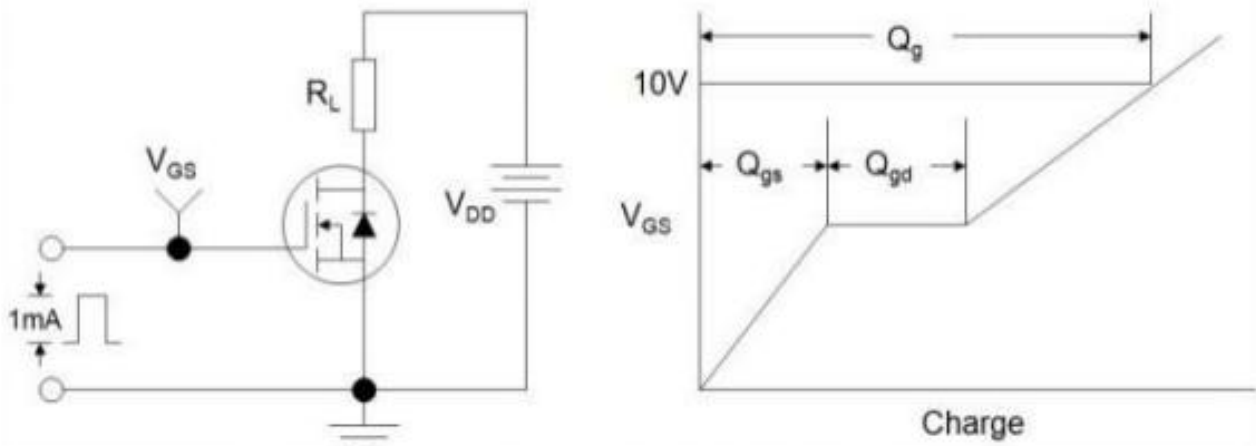


Figure B: Resistive Switching Test Circuit and Waveform

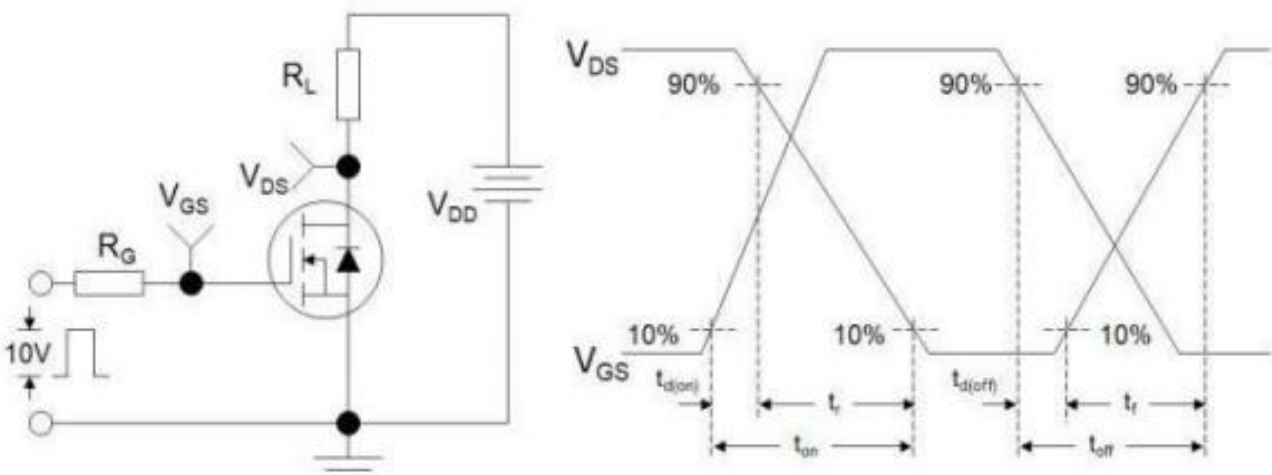
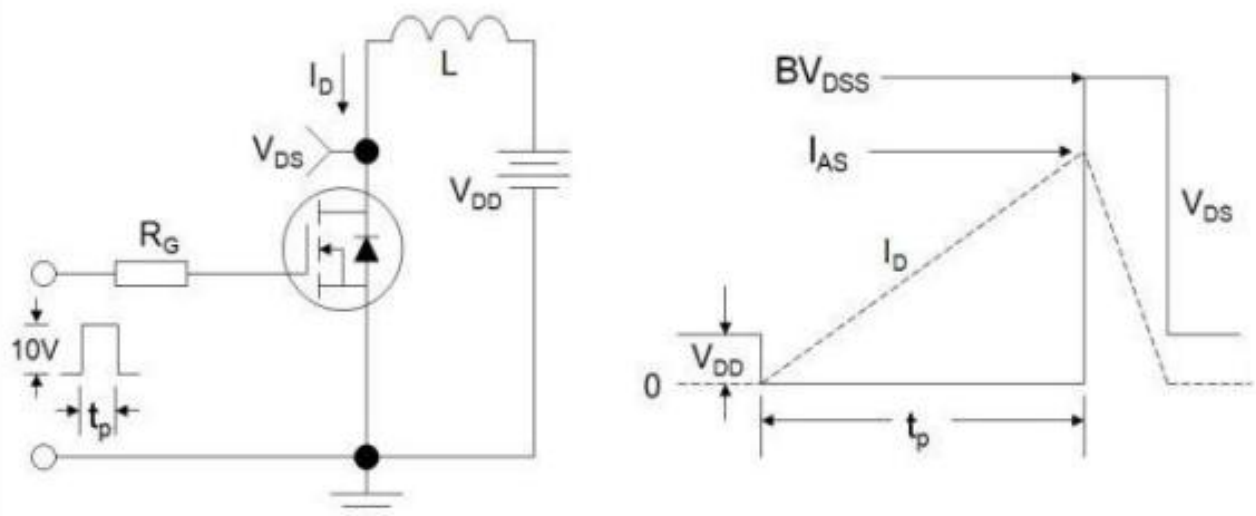
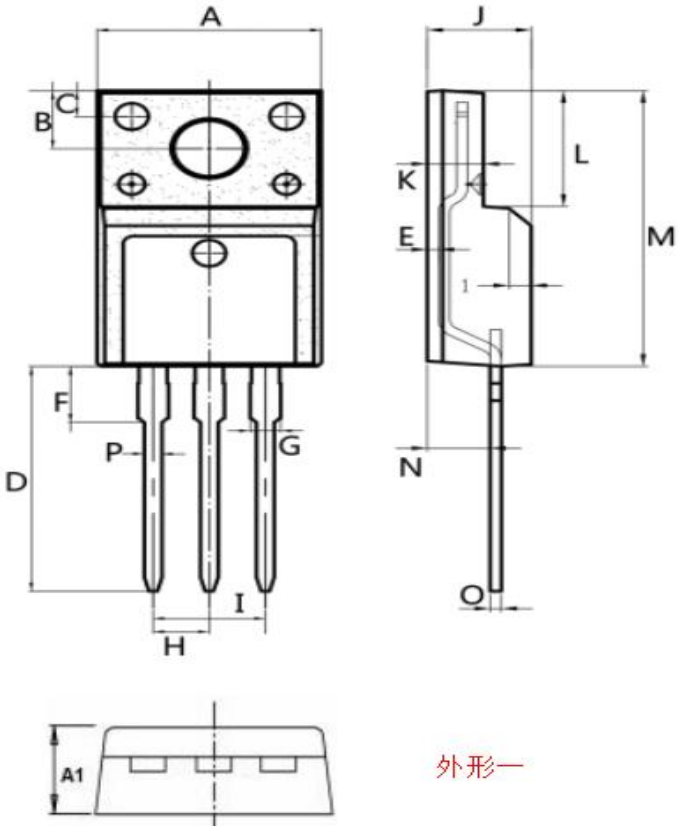
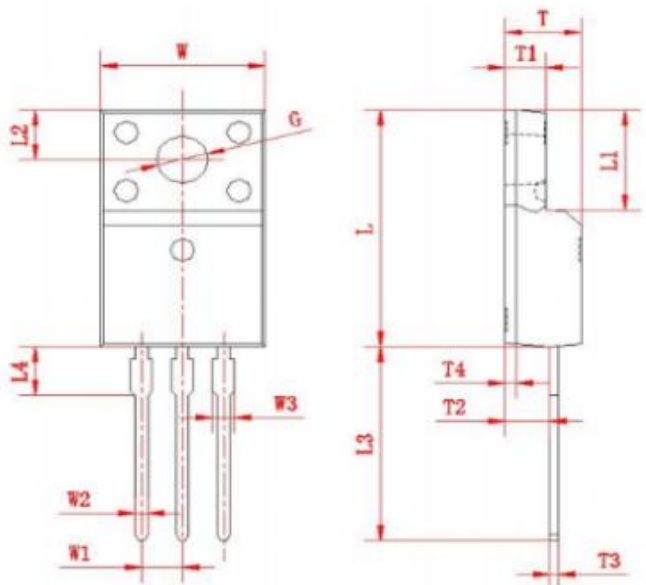


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing (TO-220F Unit: mm)

 外形一	Dim.	Min.	Max.
	A	9.95	10.36
	A1	4.5	5.0
	B	2.95	3.25
	C	1.25	1.45
	D	12.60	13.60
	E	0.40	0.60
	F	2.8	3.5
	G	1.30	1.45
	H	(2.54)	
	I	(5.08)	
	J	4.60	4.75
	K	2.45	2.65
	L	6.5	6.8
	M	15.4	16.0
	N	2.25	3.05
	O	0.45	0.55
	P	0.70	0.90
All Dimensions in millimeter			

 外形二	Dim.	Min.	Max.
	W	9.95	10.36
	W1	(2.54)	
	W2	0.70	0.90
	W3	1.25	1.47
	L	15.67	16.07
	L1	6.48	6.88
	L2	3.2	3.4
	L3	12.6	13.6
	L4	(3.23)	
	T	4.50	4.90
	T1	2.34	2.74
	T2	2.25	2.95
	T3	0.45	0.60
	T4	(0.70)	
	G	3.08	3.28
All Dimensions in millimeter			

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