

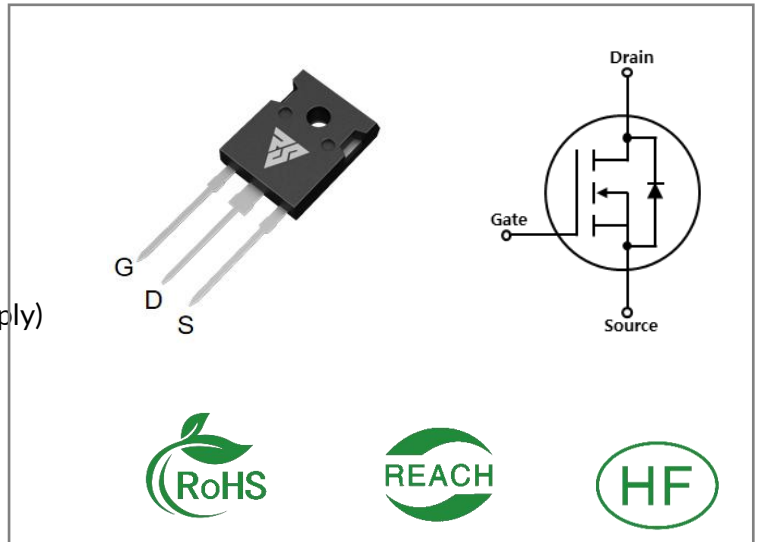
ID	$R_{DS(ON)}$ (Typ)	VDSS
68A	35mΩ	650V

Applications:

- TV and PC Power
- Adopter and Lighting
- Telecom and UPS(Uninterruptible Power Supply)

Features:

- Low gate charge
- Low $R_{DS(on)}$ per chip area(Low FOM)
- Very low switching and conduction loss
- Extremely high commutation ruggedness
- Ultra fast body diode



Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSF65R041W	T0-247	RSF65R041W	Tube	30 PCS

Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	RSF65R041W	Units
VDSS	Drain-to-Source Voltage	650	V
ID	Continuous Drain Current $T_C = 25^\circ\text{C}$ (Note*1)	68	A
ID	Continuous Drain Current $T_C = 100^\circ\text{C}$ (Note*1)	43	
IDM	Pulsed Drain Current (Note*2)	204	
PD	Power Dissipation	500	W
VGS	Gate- to- Source Voltage	± 30	V
EAS	Single Pulse Avalanche Energy $I_{AS} = 13A, V_{DD} = 50V, I_D = I_{AR}, T_j = 25^\circ\text{C}$	2100	mJ
dv/dt	MOSFET dv/ dt ruggedness $V_{DS} = 0 \dots 400V$	50	V/ns
dv/dt	Reverse diode dv/dt $V_{DS} = 0 \dots 400V, T_j = 25^\circ\text{C}, I_{SD} \leq I_D$	15	V/ns
TL TPKG	Maximum Temperature for Soldering	300	$^\circ\text{C}$
	Leads at 0.063in(1.6mm) from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

REV:P-B01-08-2025

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Thermal Resistance

Symbol	Parameter	RSF65R041W	Units	Test Conditions
R θ JC	Junction-to-Case	0.25	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 °C
R θ JA	Junction-to- Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650	--	--	V	VGS=0V ID=0.25mA
IDSS	Drain- to- Source Leakage Current	--	--	20	μA	VDS=650V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	35	40	mΩ	VGS=10V ID=34A
VGS(TH)	Gate Threshold Voltage	3	4	5	V	VGS=VDS ID=0.25mA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	137	--	nS	VDD=325V ID=68A VGS=10V RG=25Ω
trise	Rise Time	--	177	--		
td(OFF)	Turn- OFF Delay Time	--	365	--		
tfall	Fall Time	--	22	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	7570	--	pF	VGS=0V VDS=100V f=100KHz
Coss	Output Capacitance	--	260	--		
Crss	Reverse Transfer Capacitance	--	2.37	--		
Qg	Total Gate Charge	--	156	--	nC	VDS=480V ID=68A VGS=10V
Qgs	Gate- to- Source Charge	--	48	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	64	--		
RG	Gate resistance	--	2.6	--	Ω	f=1MHz ID=0A(open drain)

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	68	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	204	A	
VSD	Diode Forward Voltage	--	--	1.4	V	ISD=68A VGS=0V
trr	Reverse Recovery Time	--	222	--	nS	VDD=100V ISD=68A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	2.03	--	μC	
Irr	Reverse recovery current	--	18.3	--	A	

Notes:

* 1.limited by Tj,max

* 2.Pulse width limited by Tj,max

Typical Feature Curve

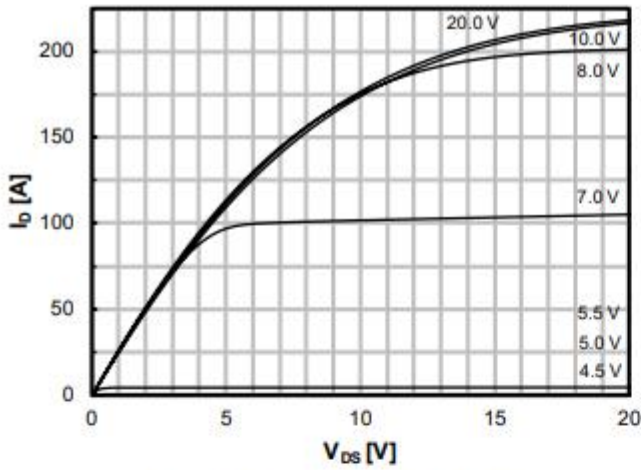


Fig. 1 Output Characteristics

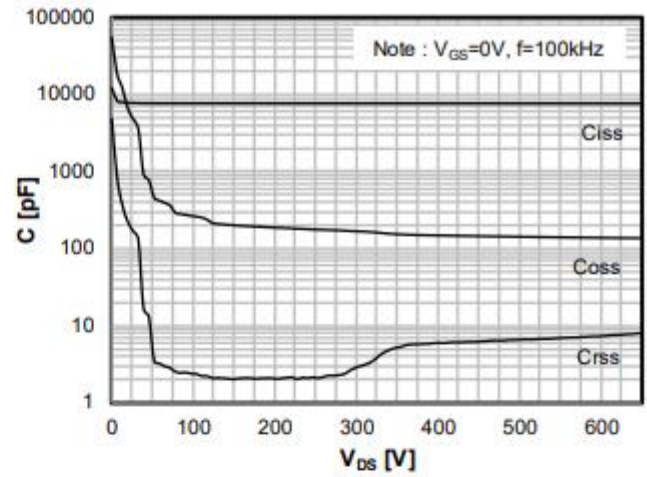


Fig. 2 Capacitances

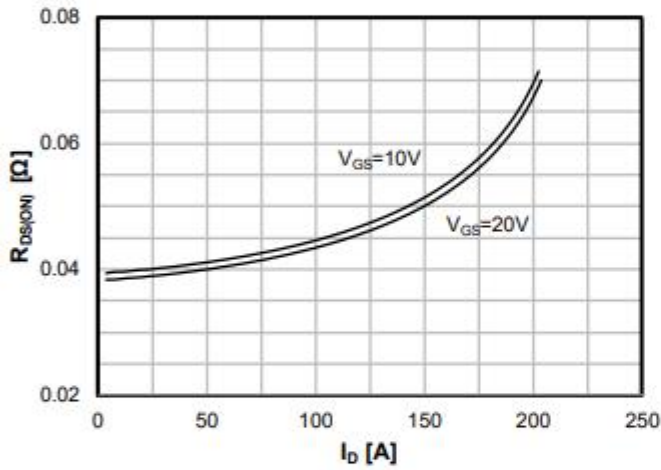


Fig. 3 On-state Resistance

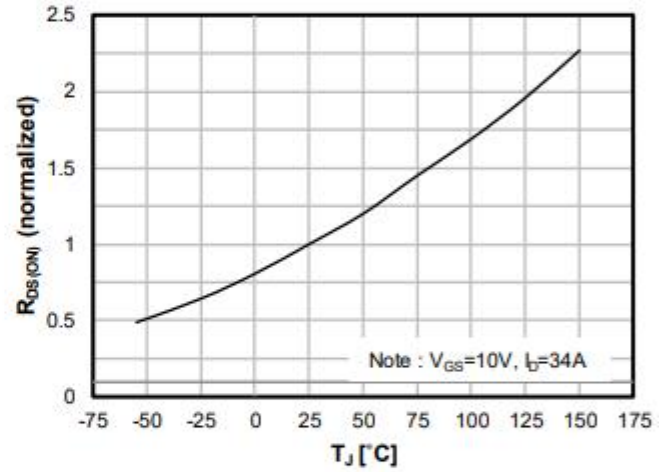


Fig. 4 On-state Resistance with Temperature

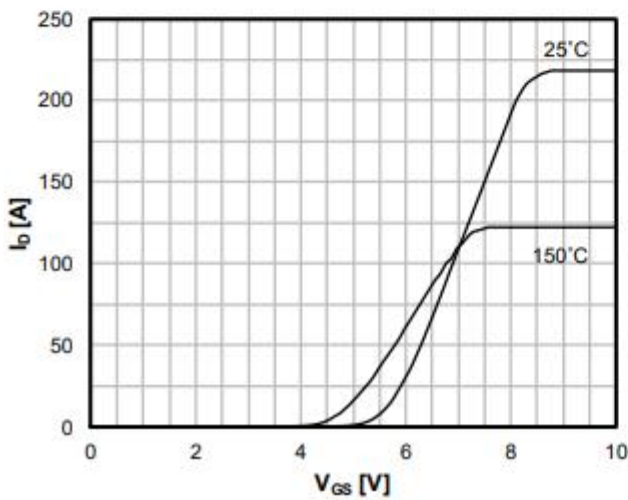


Fig. 5 Transfer Characteristics

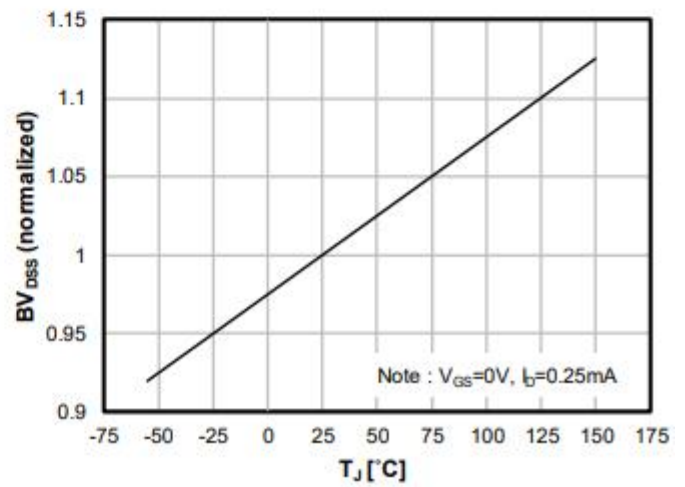
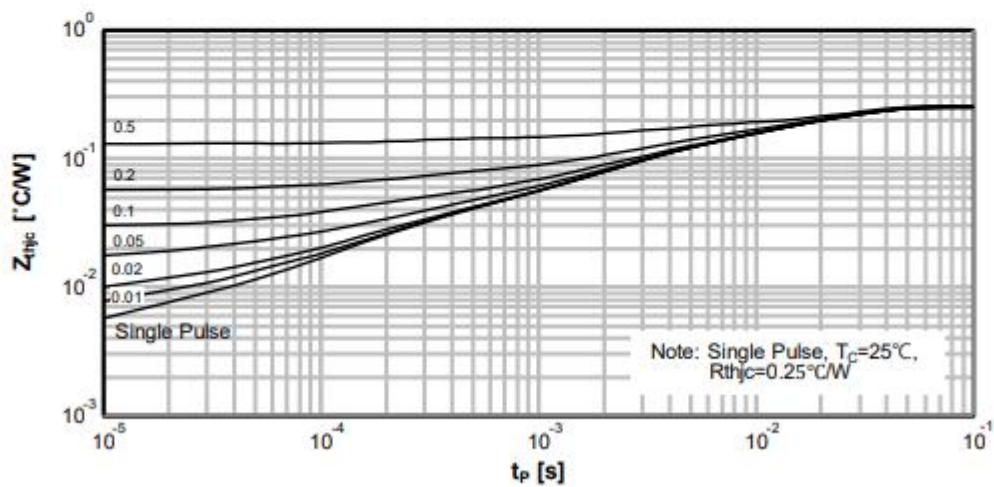
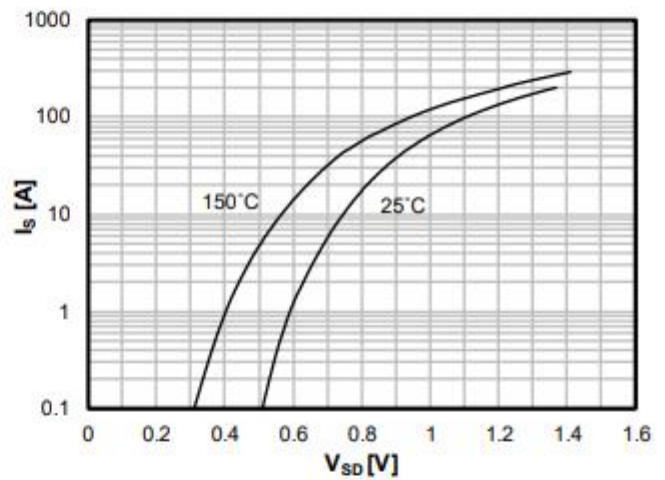
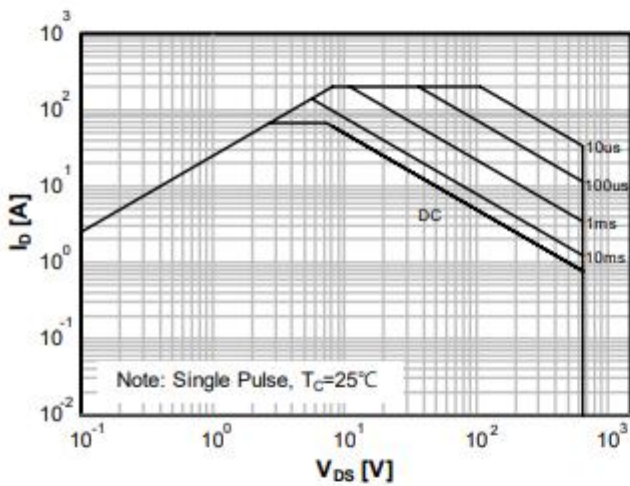
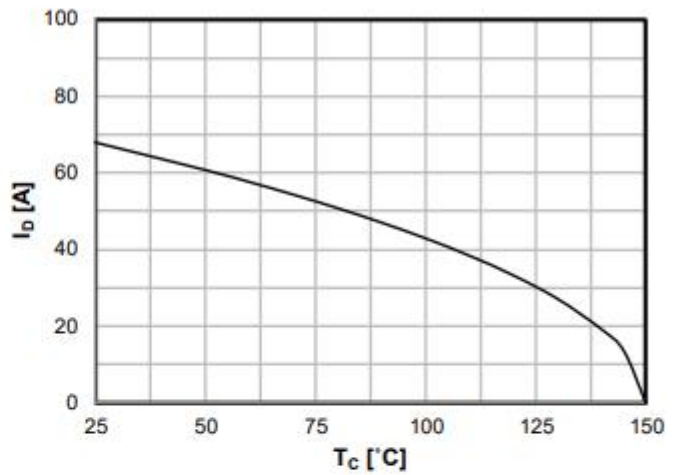
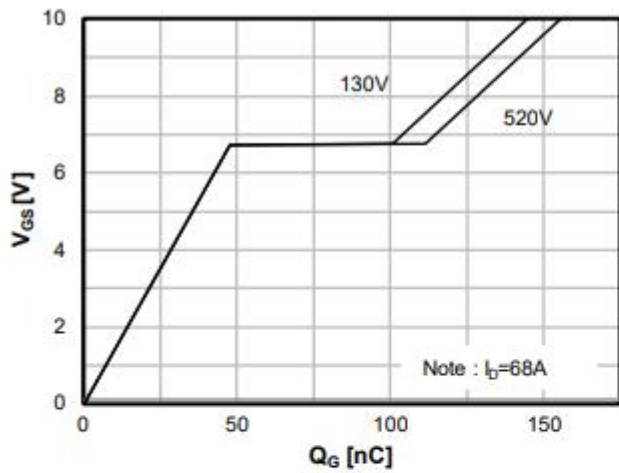


Fig. 6 Breakdown Voltage with Temperature



Test Circuits and Waveforms

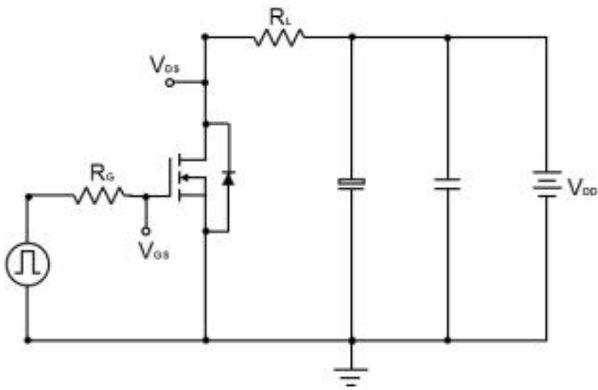


Fig. 12 Test circuit for resistive load switching times

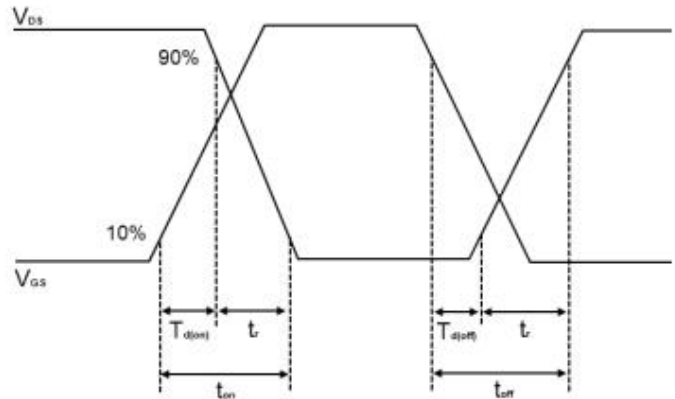


Fig. 13 Switching times waveform

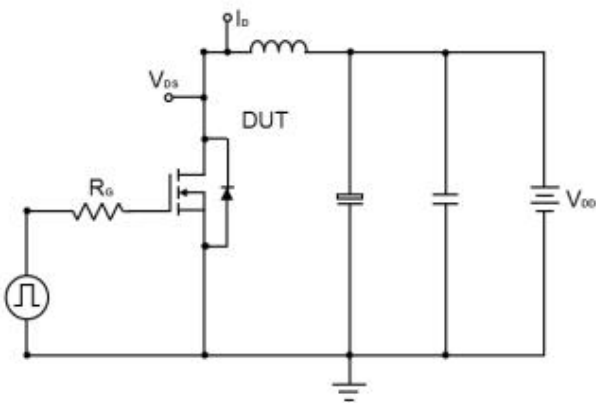


Fig. 14 Test circuit for unclamped inductive load

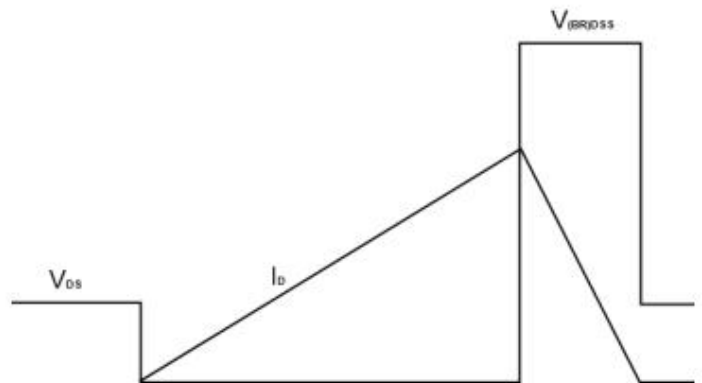


Fig. 15 Unclamped inductive waveform

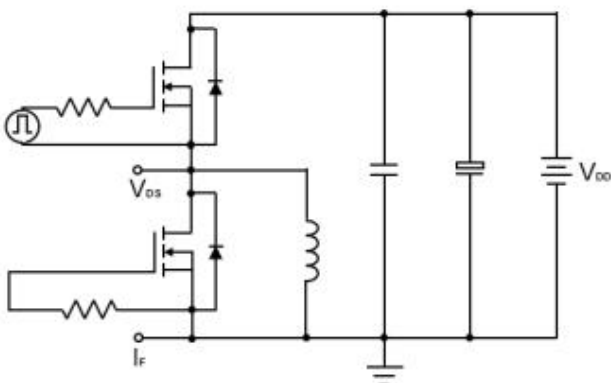


Fig. 16 Test circuit for diode characteristics

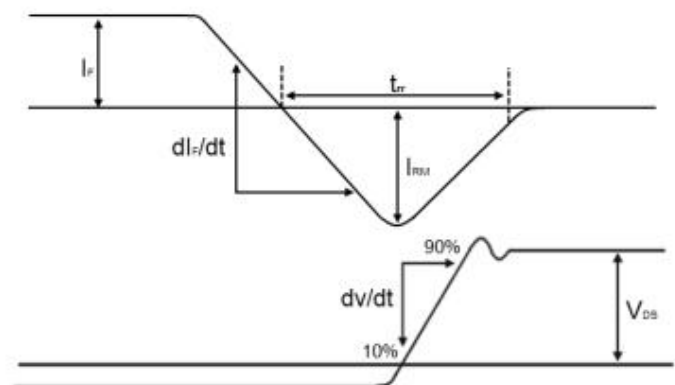
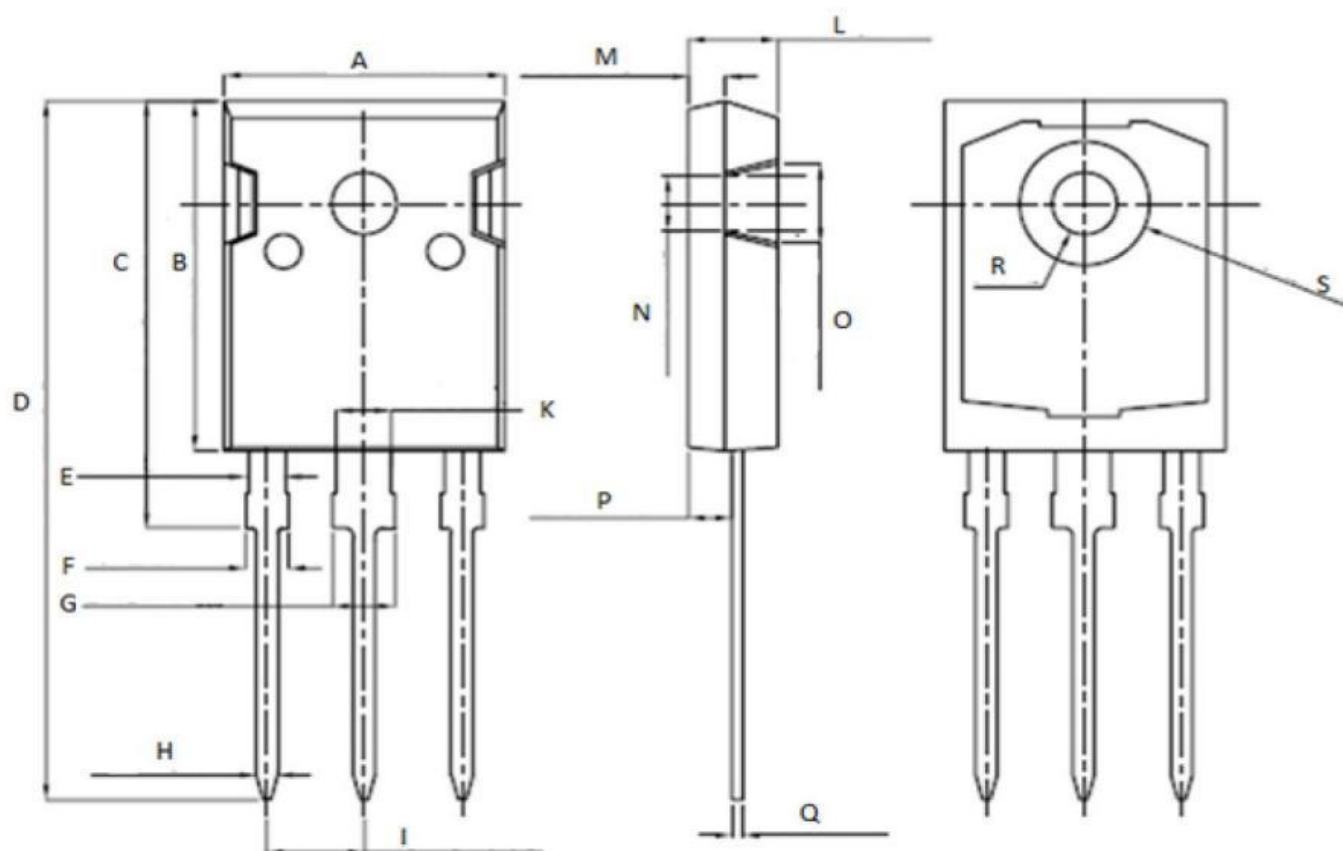


Fig. 17 Diode recovery waveform

Package outline drawing(TO-247 Unit: mm)

TO-247



Unit: mm		
Symbol	Min.	Max.
A	15.95	16.25
B	20.85	21.25
C	20.95	21.35
D	40.5	40.9
E	1.9	2.1
F	2.1	2.25
G	3.1	3.25
H	1.1	1.3
I	5.40	5.50

Unit: mm		
Symbol	Min.	Max.
K	2.90	3.10
L	4.90	5.30
M	1.90	2.10
N	4.50	4.70
O	5.40	5.60
P	2.29	2.49
Q	0.51	0.71
R	φ 3.5	φ 3.7
S	φ 7.1	φ 7.3

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