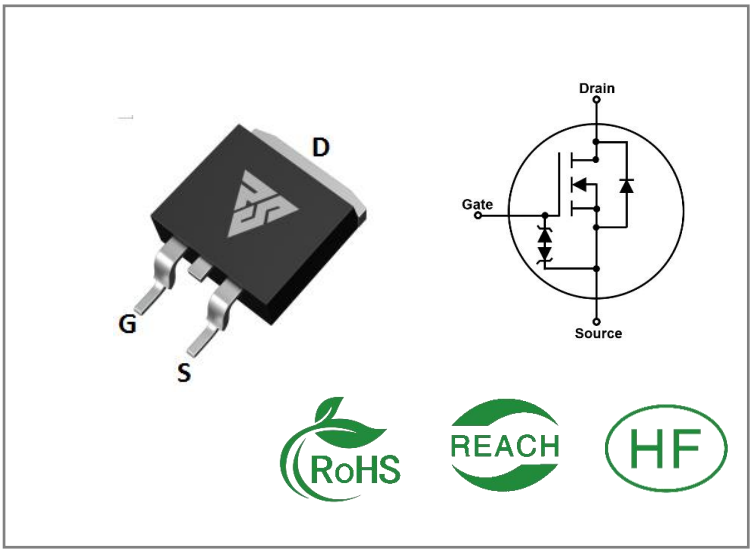
ID	R_{DS}(ON)(MAX)	VDSS
20A	250mΩ	800V



Applications:

- LED Lighting
- Telecom
- UPS(Uninterruptible Power Supply)
- SMPS(Switch Mode Power Supply)

Features:

- Excellent ESD robustness
- Excellent high commutation ruggedness
- Low RDS(on) per chip area(Low FOM)
- Low gate charge

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSE80R250S	T0-263	RSE80R250S	Tape&reel	800 PCS

Absolute Maximun Ratings Tc= 25℃ unless otherwise specified

Symbol	Parameter	RSE80R250S	Units
VDSS	Drain-to-Source Voltage	800	V
ID	Continuous Drain Current TC=25℃	20	A
ID	Continuous Drain Current TC=100℃	12.5	
IDM	Pulsed Drain Current (Note*1)	60	
PD	Power Dissipation	139	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L=30mH,VDD = 50V, ID=IAS，Tj=25℃	246	mJ
dv/dt	MOSFET dv/ dt ruggedness VDS = 0...400V	50	V/ns
dv/dt	Reverse diode dv/dt VDS = 0...400V, Tj=25℃, ISD≤ID	15	V/ns
TL TPKG	Maximum Temperature for Soldering	300	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RSE80R250S	Units	Test Conditions
RθJC	Junction-to-Case	0.9	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to- Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	800	--	--	V	VGS=0V ID=0.25mA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=800V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	1	μA	VGS=20V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-1		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	220	250	mΩ	VGS=10V ID=10A
VGS(TH)	Gate Threshold Voltage	3	4	5	V	VGS=VDS ID=0.25mA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	27	--	nS	VDS=400V ID=10A RG=4.7Ω
trise	Rise Time	--	18	--		
td(OFF)	Turn- OFF Delay Time	--	69	--		
tfall	Fall Time	--	15	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1996	--	pF	VGS=0V VDS=50V f=1.0MHz
Coss	Output Capacitance	--	75	--		
Crss	Reverse Transfer Capacitance	--	4	--		
Qg	Total Gate Charge	--	41	--	nC	VDS=600V ID=10A VGS=10V
Qgs	Gate- to- Source Charge	--	11	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	15	--		
RG	Gate resistance	--	4.0	--	Ω	f = 1MHz ID= 0A(open drain)

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	20	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	80	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=10A,VGS=0V
trr	Reverse Recovery Time	--	365	--	nS	VDD=600V IS=10A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	4.2	--	μC	
Irr	Reverse recovery current	--	22	--	A	

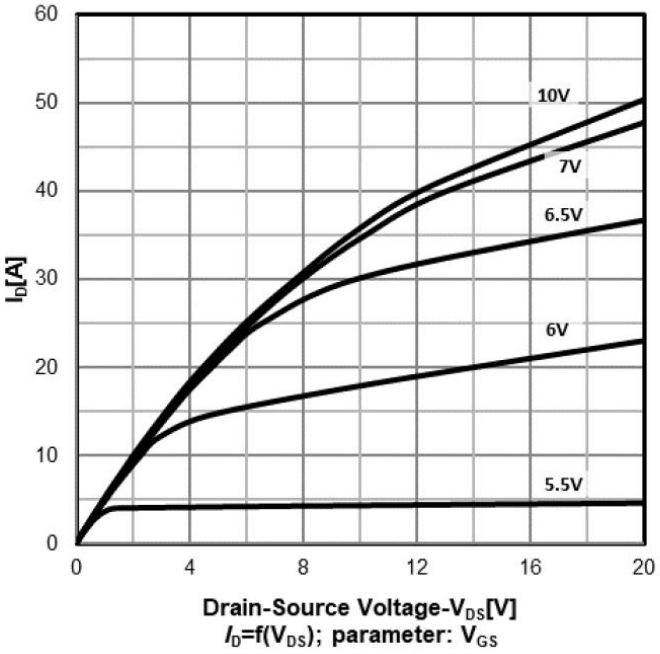
Notes:

* 1. Repetitive rating; pulse width limited by maximum junction temperature.

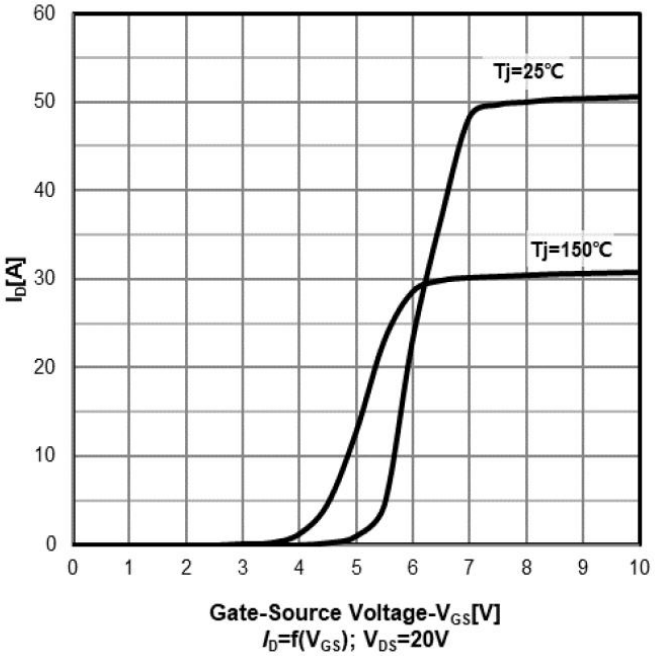
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

Typical Feature Curve

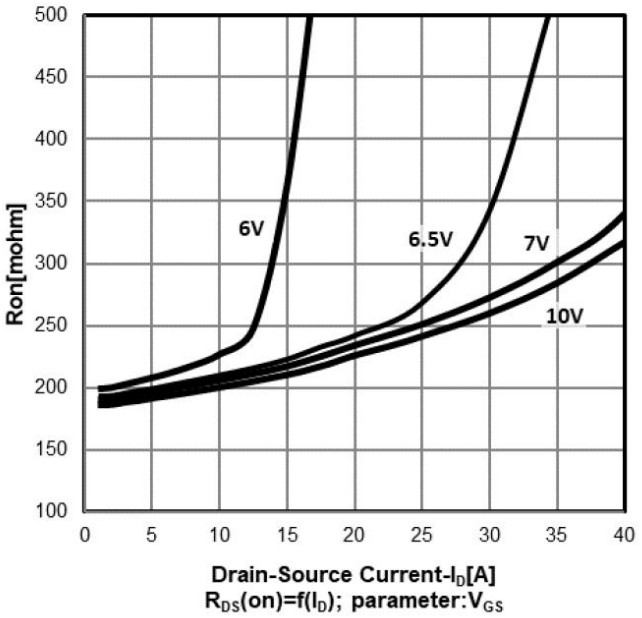
Typ. output characteristics T_j=25 ℃



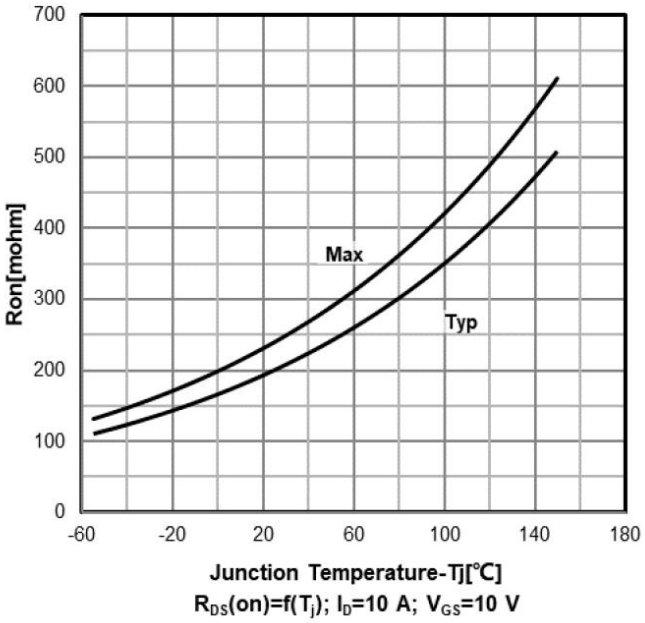
Typ. transfer characteristics



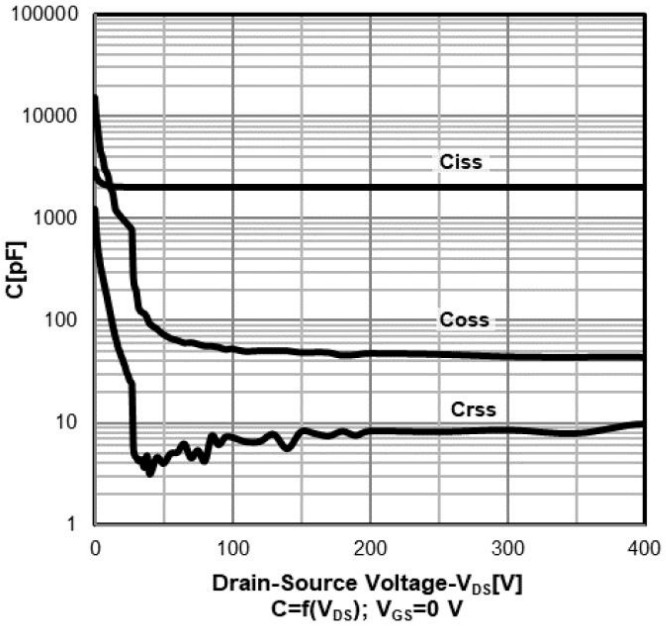
Typ. drain-source on-state resistance



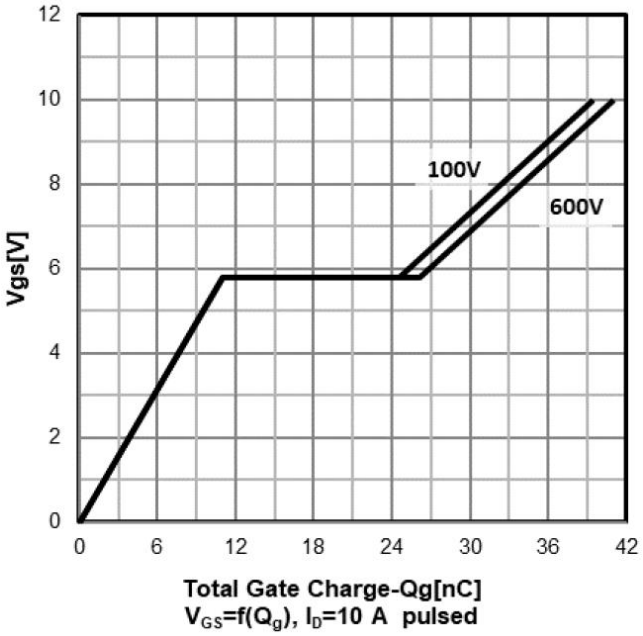
On resistance vs temperature



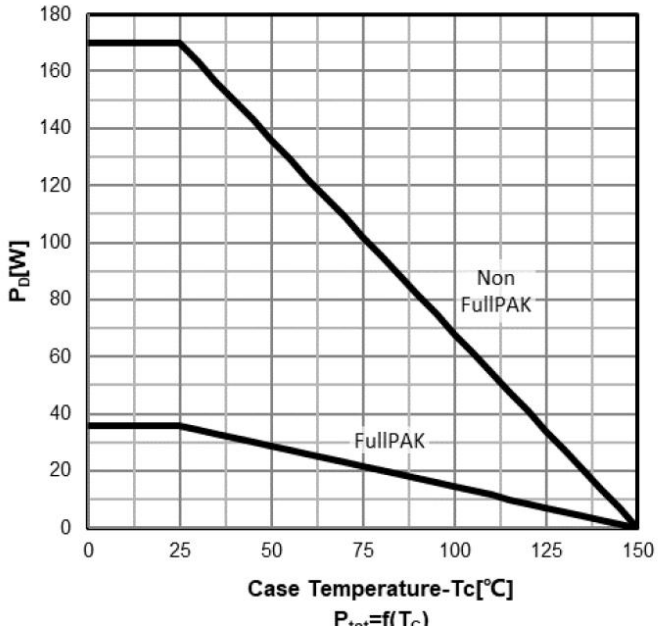
Typ. capacitances



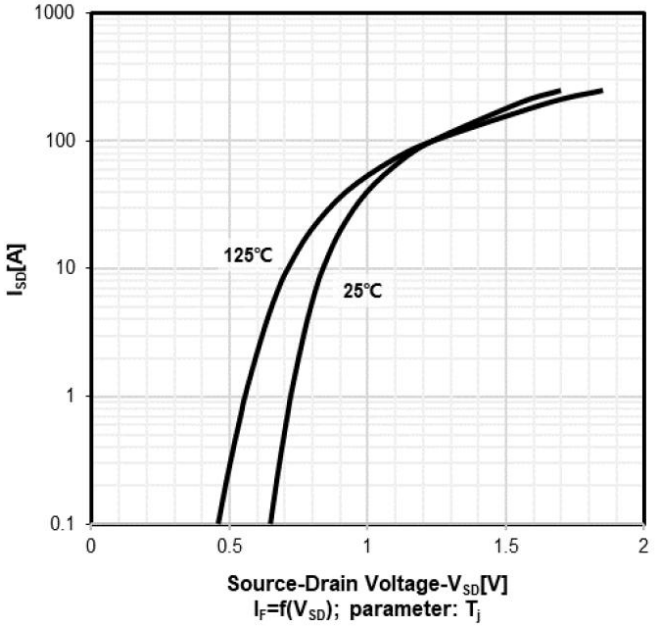
Typ. gate charge characteristics



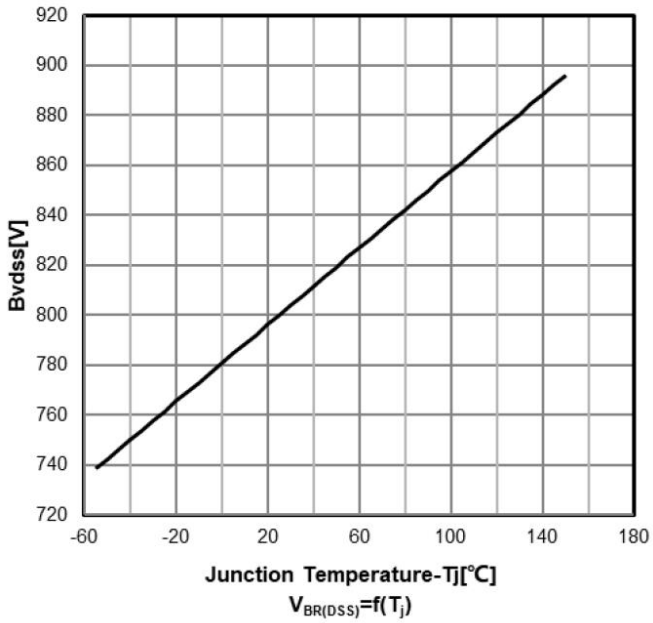
Power dissipation



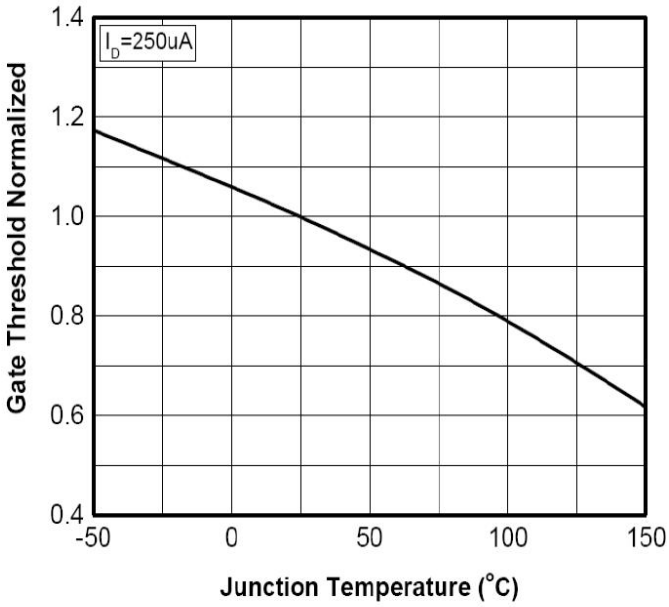
Forward characteristics of reverse diode



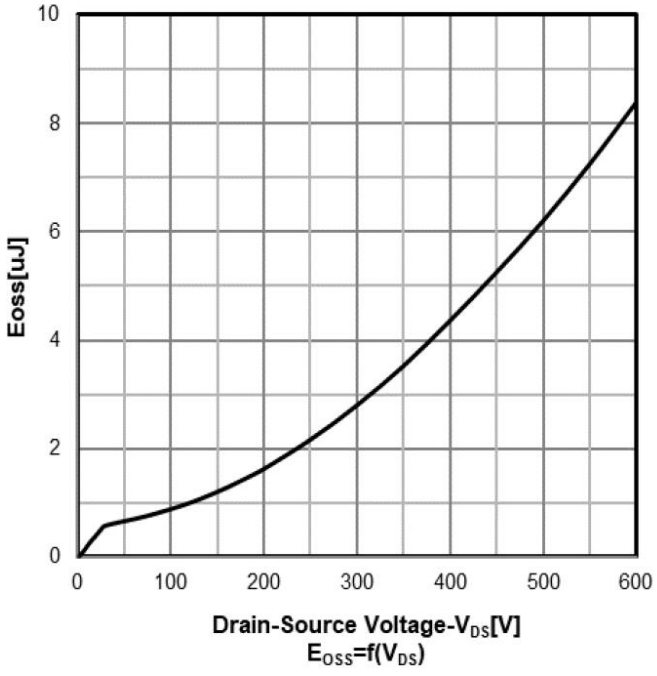
Drain-source breakdown voltage



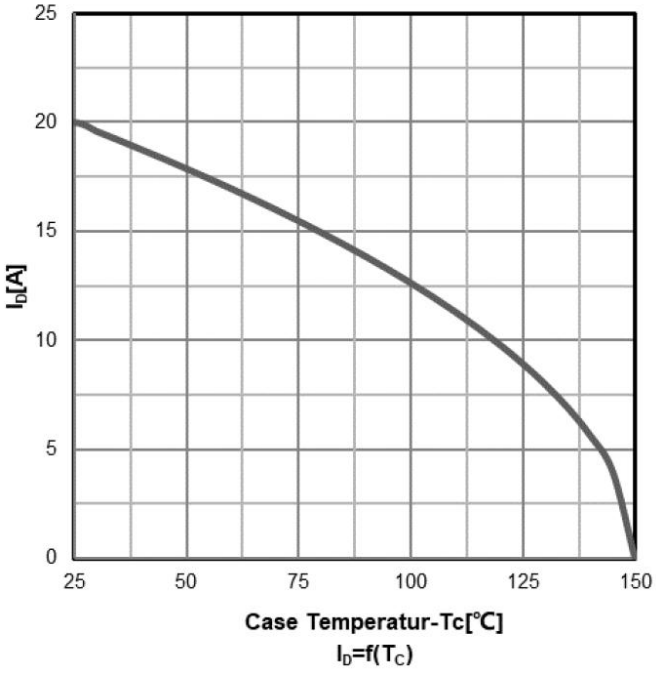
Normalized $V_{GS(th)}$ characteristics



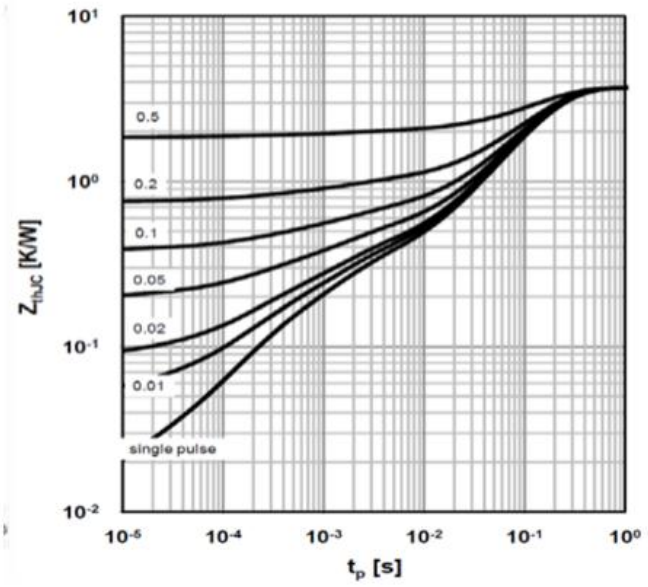
Coss stored energy



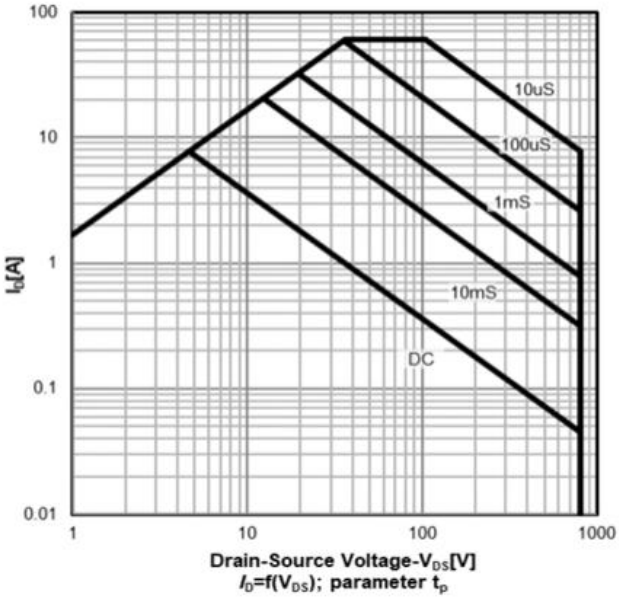
Drain current vs temperature



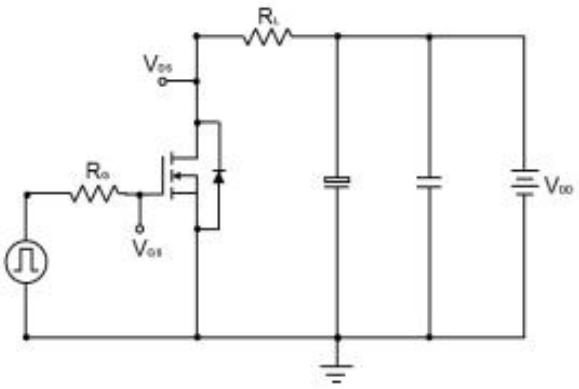
Max. transient thermal impedance
parameter: D=tp/T; TO-220FullPAK



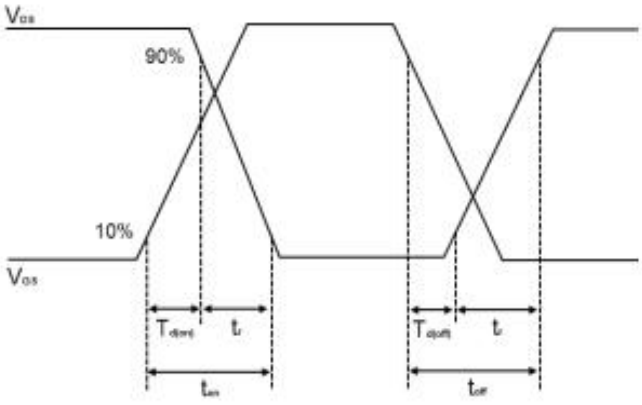
Safe operating area TC=25 ℃
TO-220FullPAK



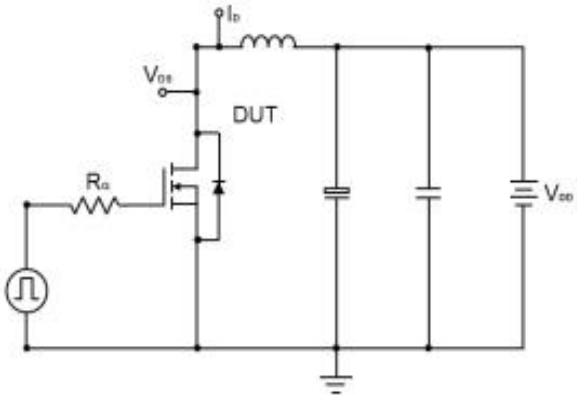
Test Circuits and Waveforms



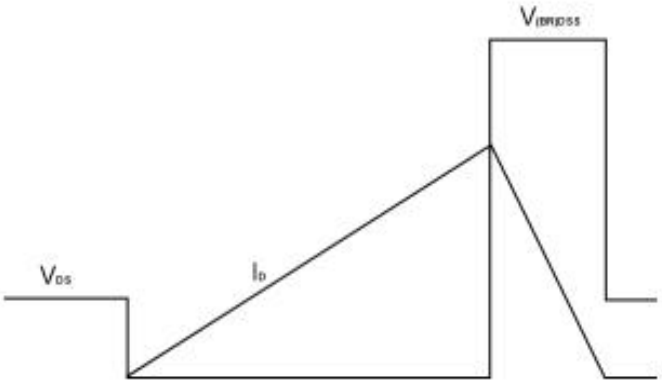
Test circuit for resistive load switching times



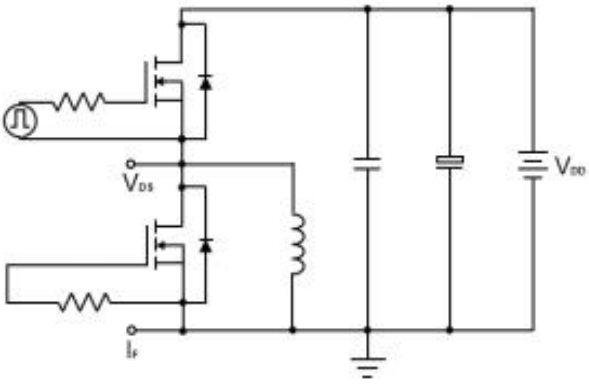
Switching times waveform



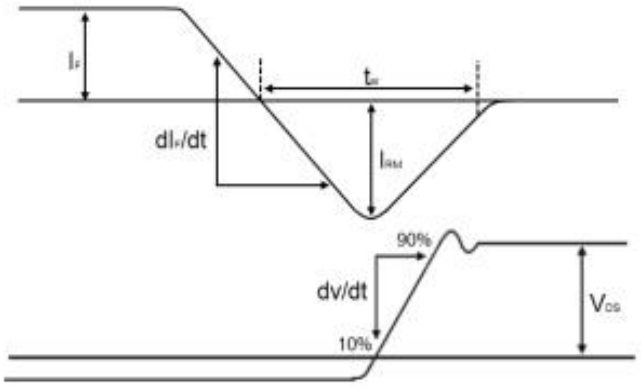
Test circuit for unclamped inductive load



Unclamped inductive waveform

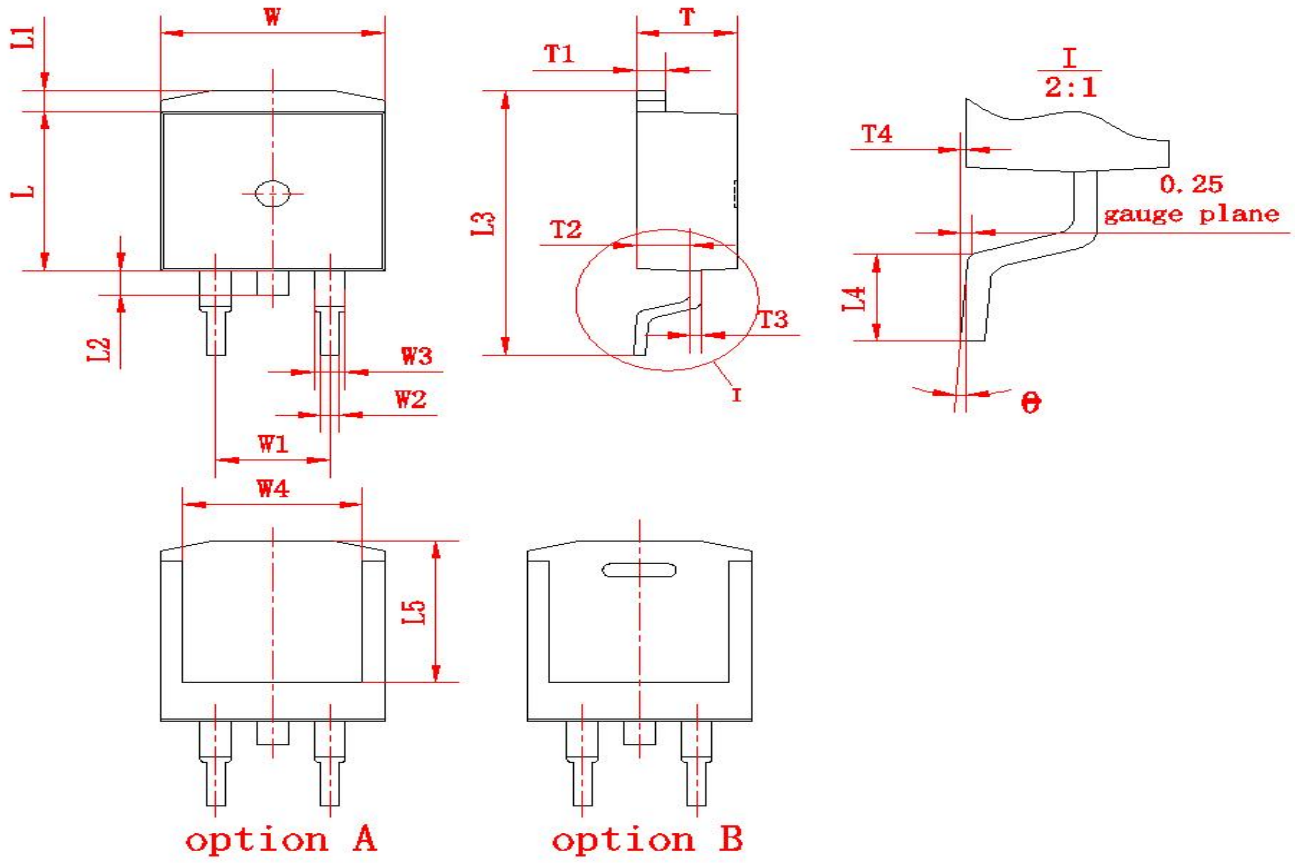


Test circuit for diode characteristics



Diode recovery waveform

Package outline drawing(TO-263 Unit: mm)



（单位：mm）

符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	9.80	10.20	L1	1.00	1.40	T1	1.20	1.40
W1	(5.08)		L2	1.20	1.60	T2	2.20	2.60
W2	0.70	0.95	L3	15.00	15.60	T3	0.45	0.65
W3	1.17	1.62	L4	2.20	2.80	T4	0	0.25
W4	(8.0)		L5	(8.2)		θ	0°	8°
L	9.00	9.40	T	4.30	4.70			

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