

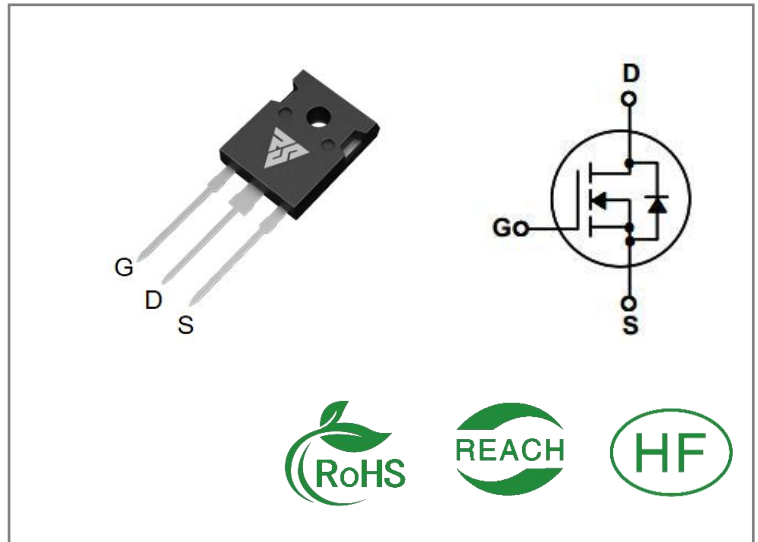
ID	$R_{DS(ON)}$ (Typ)	VDSS
55A	57mΩ	600V

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC-DC Switching Power Supply

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability
- Fast Recovery Time



Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSF60T070W	T0-247-3	RSF60T070W	Tube	30 PCS

Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	RSF60T070W	Units
VDSS	Drain-to-Source Voltage	600	V
ID	Continuous Drain Current $T_C=25^\circ\text{C}$	55	A
ID	Continuous Drain Current $T_C=100^\circ\text{C}$	38	
IDM	Pulsed Drain Current (Note*1)	220	
PD	Power Dissipation	236	W
VGS	Gate- to- Source Voltage	± 30	V
EAS	Single Pulse Avalanche Energy IAS=4.9A, VDD = 50V, RG = 25 Ω, TC=25°C	750	mJ
dv/dt	Peak Diode Recovery dv/dt	50	V/ns
TL TPKG	Maximum Temperature for Soldering	300	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds	260	
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RSF60T070W	Units	Test Conditions
R θ JC	Junction-to-Case	0.53	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\text{C}$
R θ JA	Junction-to- Ambient	39		1 cubic foot chamber,free air.

OFF Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	600	--	--	V	VGS=0V ID=250 μA
IDSS	Drain- to- Source Leakage Current	--	--	10	μA	VDS=600V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	57	68	m Ω	VGS=10V ID=27A
VGS(TH)	Gate Threshold Voltage	3	--	5	V	VGS=VDS ID=250 μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	32	--	nS	VDS=400V ID=24A RG=2.5 Ω
trise	Rise Time	--	32	--		
td(OFF)	Turn- OFF Delay Time	--	42	--		
tfall	Fall Time	--	23	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	3421	--	pF	VGS=0V VDS=100V f=1.0MHz
Coss	Output Capacitance	--	110	--		
Crss	Reverse Transfer Capacitance	--	4.3	--		
Qg	Total Gate Charge	--	70	--	nC	VDS=480V ID=24A VGS=10V
Qgs	Gate- to- Source Charge	--	22	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	28	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	55	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	220	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=24A VGS=0V
trr	Reverse Recovery Time	--	200	--	nS	VR=300V IS=24A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	1.4	--	μC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

Typical Feature Curve

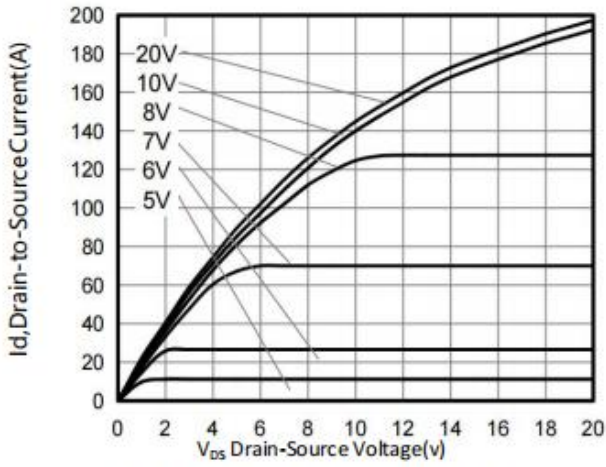


Figure1. Typical Output Characteristics

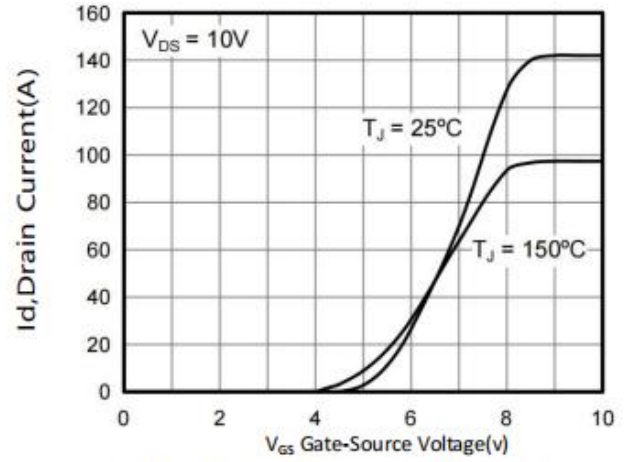


Figure2. Typical Transfer Characteristics

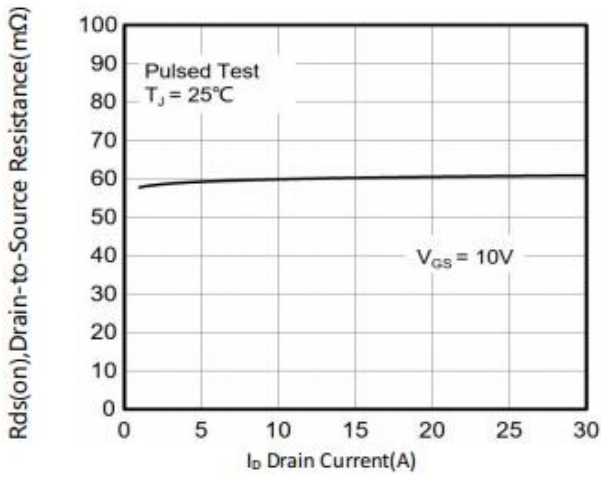


Figure3. On-Resistance versus Drain Current

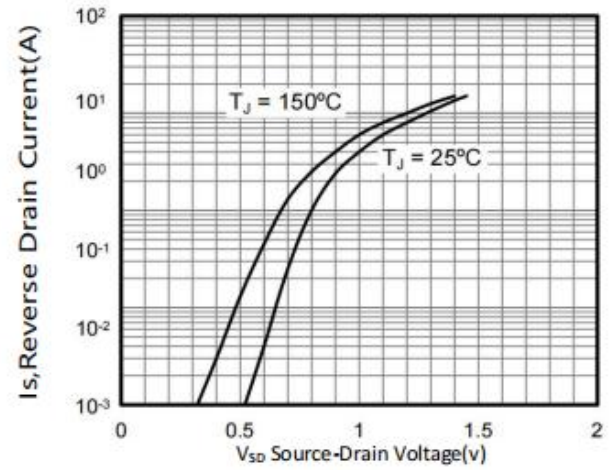


Figure4. Diode forward voltage versus Current

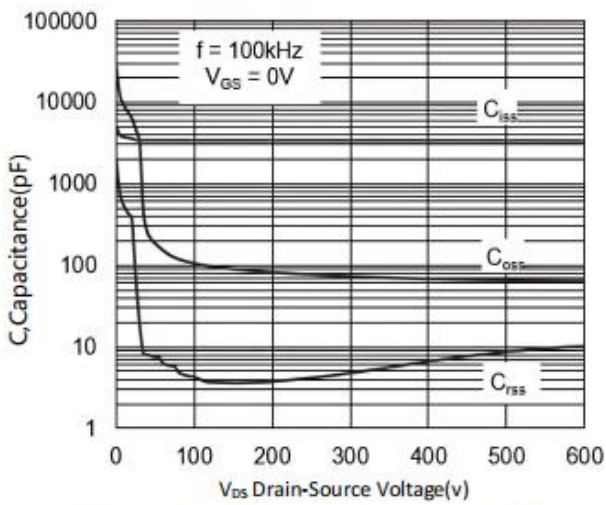


Figure5. Typical Capacitance versus VDS

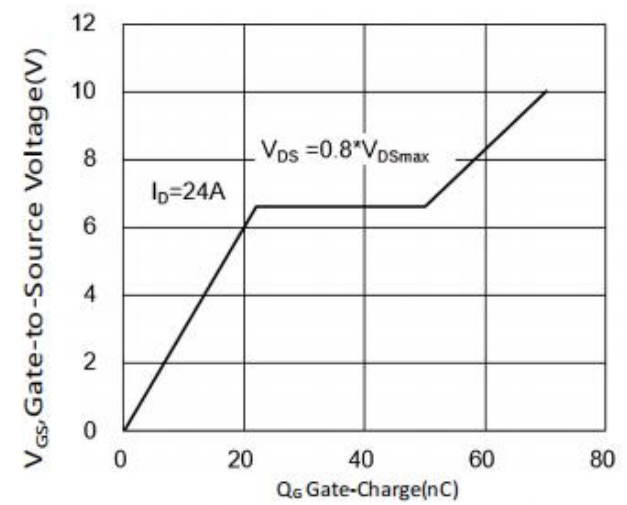


Figure6. Typical Gate Charge versus VGS

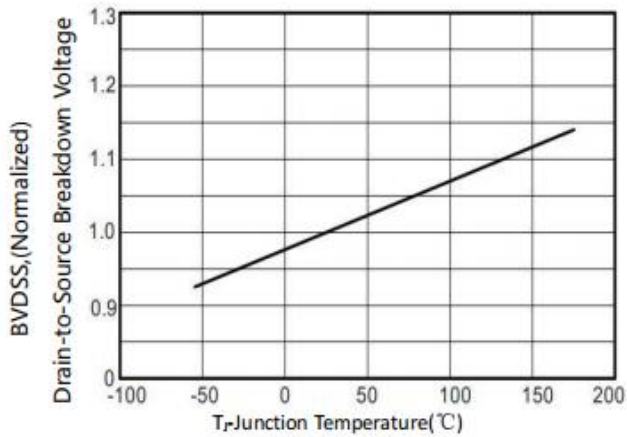


Figure7. BV_{DSS} Variation with Temperature

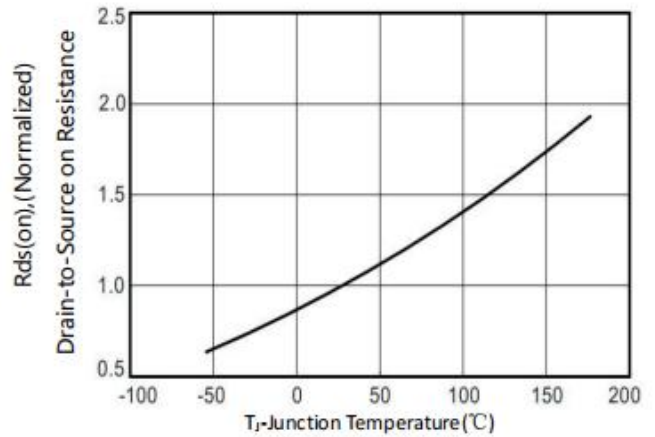
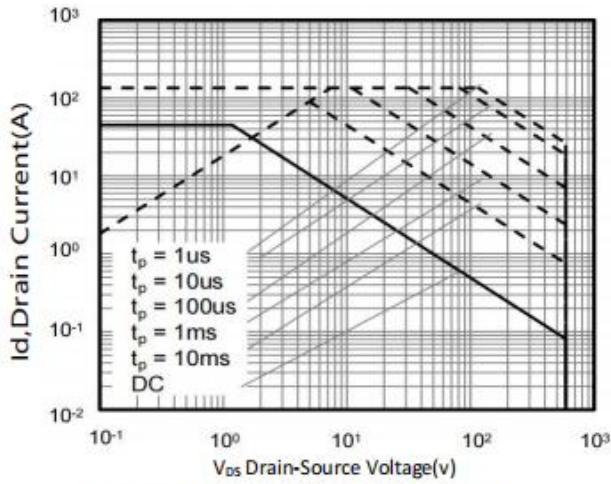
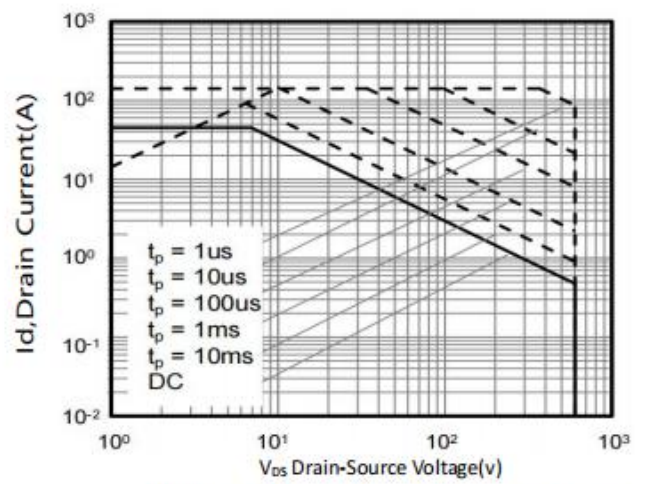


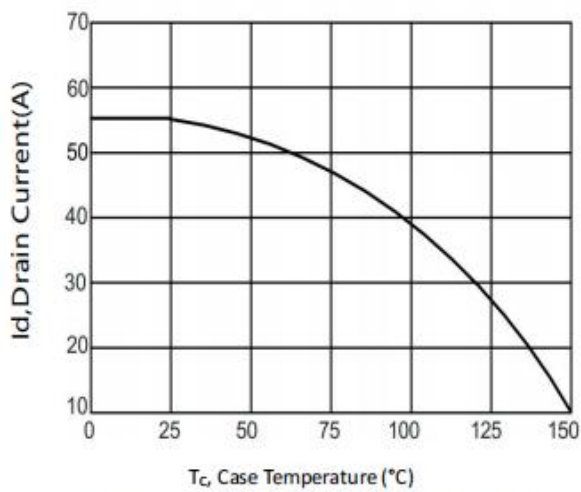
Figure8. On-Resistance Variation with Temperature



**Figure9. Maximum Safe Operating Area
TO-220F**

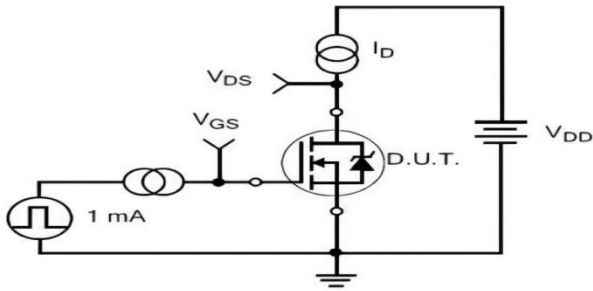


**Figure9. Maximum Safe Operating Area
TO-247/TO-263**

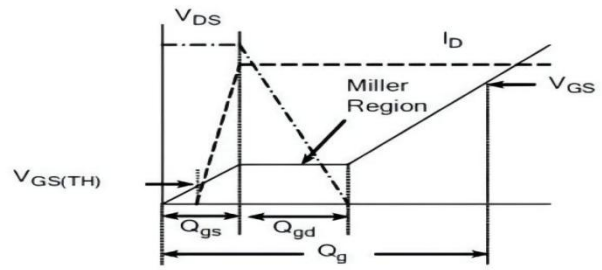


**Figure10. Maximum Continuous Drain
versus Case Temperature**

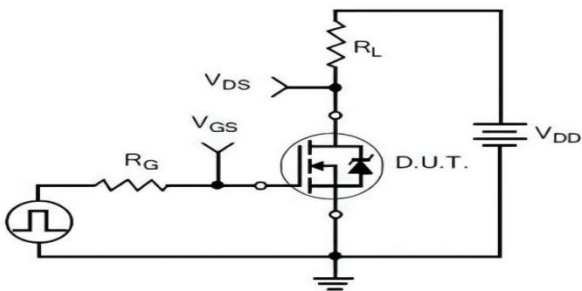
Test Circuits and Waveforms



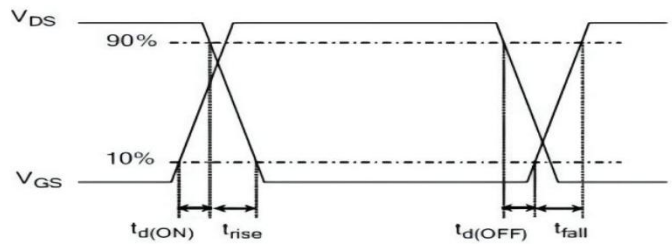
Gate Charge Test Circuit



Gate Charge Waveform

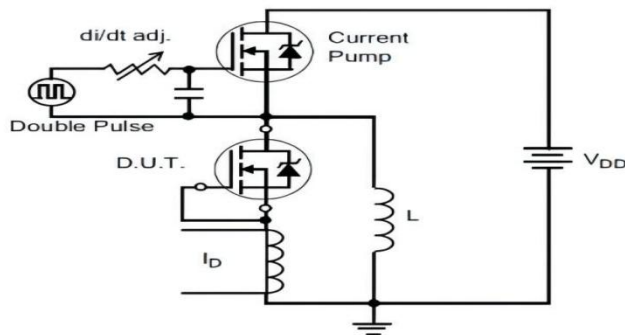


Resistive Switching Test Circuit

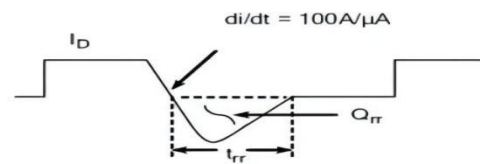


Resistive Switching Waveforms

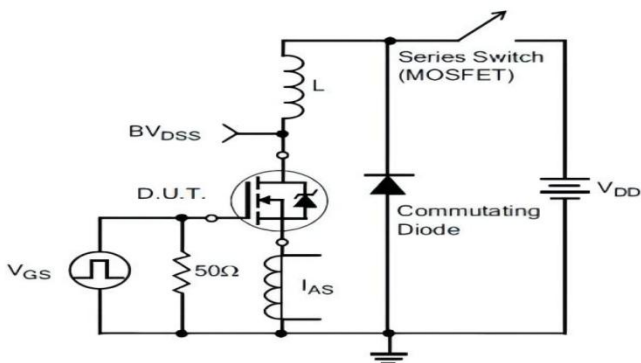
Test Circuits and Waveforms



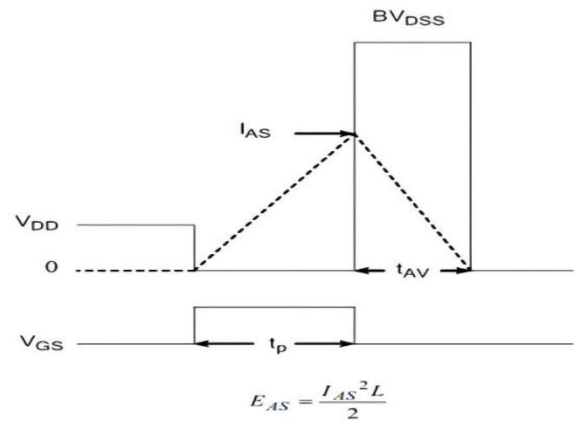
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform

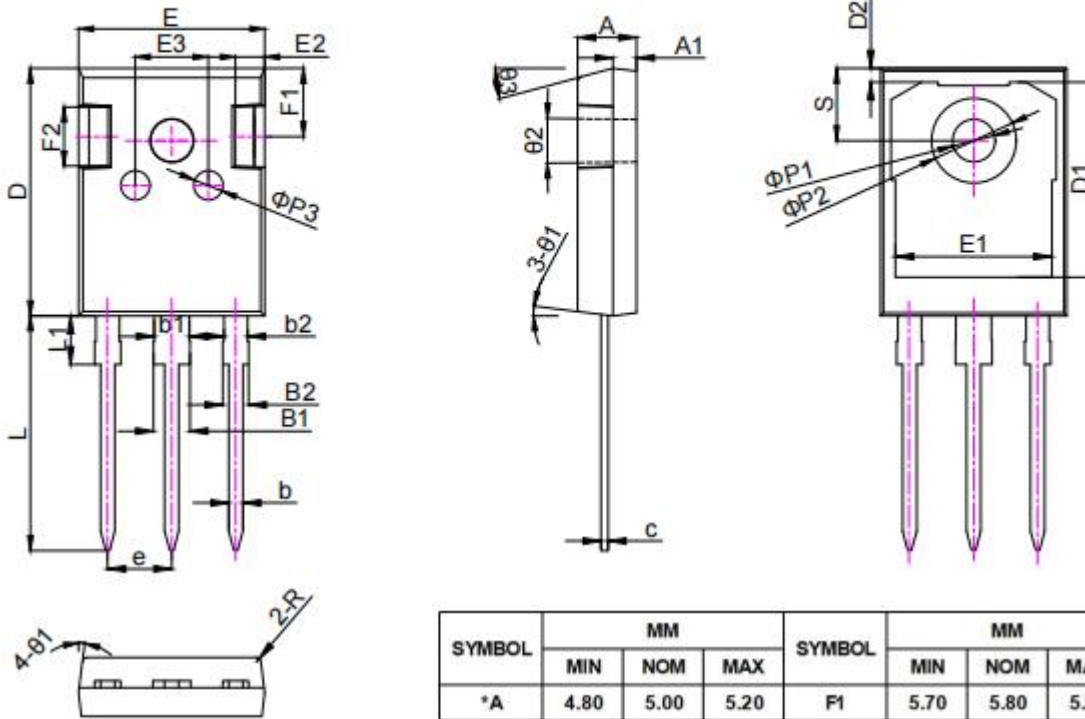


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Package outline drawing(TO-247-3 Unit: mm)



SYMBOL	MM			SYMBOL	MM		
	MIN	NOM	MAX		MIN	NOM	MAX
*A	4.80	5.00	5.20	F1	5.70	5.80	5.90
A1	1.90	2.00	2.10	F2	4.85	5.00	5.15
*b	1.10	1.20	1.30	*e	5.39	5.44	5.49
b1	2.90	3.00	3.10	*L	19.72	19.92	20.12
b2	1.95	2.00	2.05	*L1	4.03	4.13	4.23
*B1	3.00	3.10	3.20	θ1	5°	7°	9°
*B2	2.00	2.10	2.20	θ2	1°	2°	3°
*c	0.50	0.6	0.70	θ3	13°	15°	17°
*D	20.80	21	21.20	*ΦP1	3.50	3.60	3.70
D1	16.40	16.55	16.70	ΦP2	7.09	7.19	7.29
D2	1.07	1.17	1.27	ΦP3	2.40	2.50	2.60
*E	15.60	15.80	16.00	*Q1	2.31	2.41	2.51
E1	13.11	13.26	13.41	S	6.05	6.15	6.25
E2	2.40	2.50	2.60	R	0.30	0.40	0.50
E3	6.10	6.20	6.30	带*为关键检验尺寸			

注:
1.表面粗糙度 $R_a \leq 1.14 \pm 0.20 \mu m$
2.带*为关键检验尺寸

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