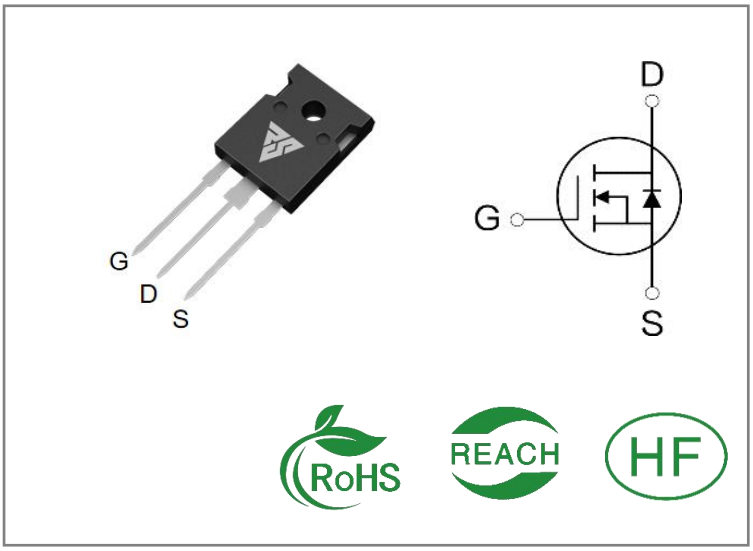
| ID | $R_{DS}$(ON)(Typ ) | VDSS |
|---|---|---|
| 3A | 5.5Ω | 1500V |




## Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

## Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

## Ordering Information

| Part Number | Package | Marking | Packing | Qty. |
|---|---|---|---|---|
| RS3N150W | T0-247 | RS3N150W | Tube | 30 PCS |

## Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

| Symbol | Parameter | RS3N150W | Units |
|---|---|---|---|
| VDSS | Drain-to-Source Voltage | 1500 | V |
| ID | Continuous Drain Current TC=25℃ | 3 | A |
| IDM | Pulsed Drain Current (Note*1) | 12 | |
| PD | Power Dissipation | 368 | W |
| VGS | Gate- to- Source Voltage | ±30 | V |
| EAS | Single Pulse Avalanche Engergy<br>L = 10mH, VDD = 50V, RG = 25 Ω | 88 | mJ |
| TL TPKG | Maximum Temperature for Soldering | 300<br>260 | ℃ |
| | Leads at 0.063in(1.6mm)from Case for 10 seconds<br>Package Body for 10 seconds | | |
| TJ and TSTG | Operating Junction and Storage Temperature Range | -55 to 150 | |

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.


Copyright Reasunos

## Thermal Resistance

| Symbol | Parameter | RS3N150W | Units | Test Conditions |
|---|---|---|---|---|
| RθJC | Junction-to-Case | 0.34 | ℃/ W | Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃ |
| RθJA | Junction-to-Ambient | 62.5 | | 1 cubic foot chamber,free air. |

## OFF Characteristics TJ= 25℃ unless otherwise specified

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| BVDSS | Drain- to- source Breakdown Voltage | 1500 | -- | -- | V | VGS=0V,ID=250μA |
| IDSS | Drain- to- Source Leakage Current | -- | -- | 1 | μA | VDS=1500V,VGS=0V |
| IGSS | Gate- to- Source Forward Leakage | -- | -- | 100 | nA | VGS=30V ,VDS=0V |
| | Gate- to- Source Reverse Leakage | -- | -- | -100 | | VGS=-30V ,VDS=0V |

## ON Characteristics TJ=25℃ unless otherwise specified

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| RDS(on) | Static Drain- to- Source On-Resistance(Note*2) | -- | 5.5 | 6.5 | Ω | VGS=10V,ID=1.5A |
| VGS(TH) | Gate Threshold Voltage | 3 | -- | 5 | V | VGS=VDS,ID=250μA |

## Resistive Switching Characteristics Essentially independent of operating temperature

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| td(ON) | Turn- on Delay Time | -- | 48 | -- | nS | VDS=750V<br>ID=3A<br>RG=25Ω |
| trise | Rise Time | -- | 6 | -- | | |
| td(OFF) | Turn- OFF Delay Time | -- | 25 | -- | | |
| tfall | Fall Time | -- | 6 | -- | | |


Copyright Reasunos

**Dynamic Characteristics** Essentially independent of operating temperature

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Ciss | Input Capacitance | -- | 1275 | -- | pF | VGS=0V<br>VDS=25V<br>f=1.0MHz |
| Coss | Output Capacitance | -- | 98 | -- | | |
| Crss | Reverse Transfer Capacitance | -- | 12 | -- | | |
| Qg | Total Gate Charge | -- | 50 | -- | nC | VDS=1200V<br>ID=3A<br>VGS=10V |
| Qgs | Gate- to- Source Charge | -- | 6 | -- | | |
| Qgd | Gate-to-Drain(" Miller") Charge | -- | 25 | -- | | |

## Source- Drain Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| IS | Continuous Source Current | -- | -- | 3 | A | Integral pn- diode in MOSFET |
| ISM | Maximum Pulsed Current | -- | -- | 12 | A | |
| VSD | Diode Forward Voltage | -- | -- | 1.4 | V | IS=1.5A,VGS=0V |
| trr | Reverse Recovery Time | -- | 1060 | -- | nS | VGS=0V<br>IS=3A,di/dt=100A /μs |
| Qrr | Reverse Recovery Charge | -- | 5.4 | -- | μC | |

**Notes:**

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%


Copyright Reasunos

## Typical Feature Curve

Figure 1. Output Characteristics ($T_J$ = 25℃)

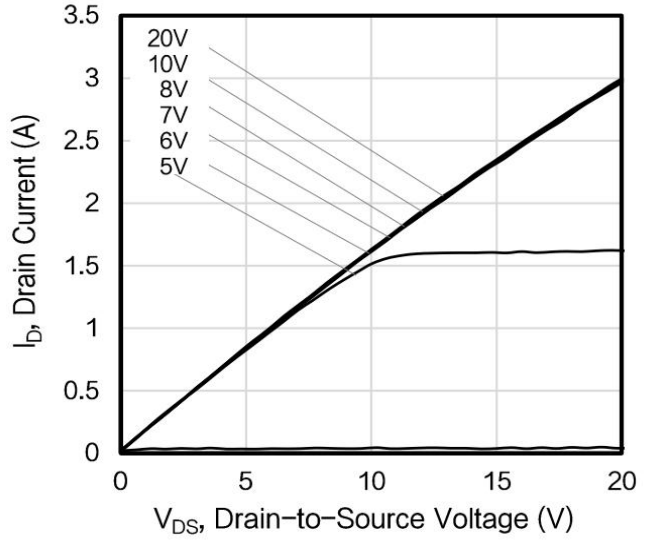



Figure 2. Body Diode Forward Voltage

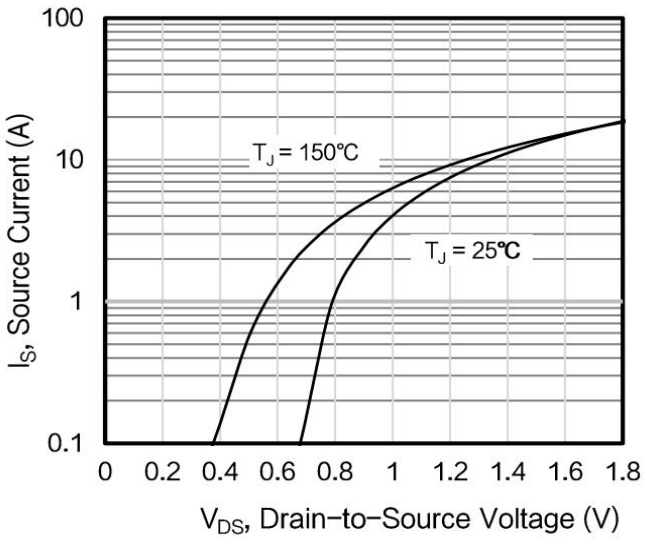



Figure 3. Drain Current vs. Temperature

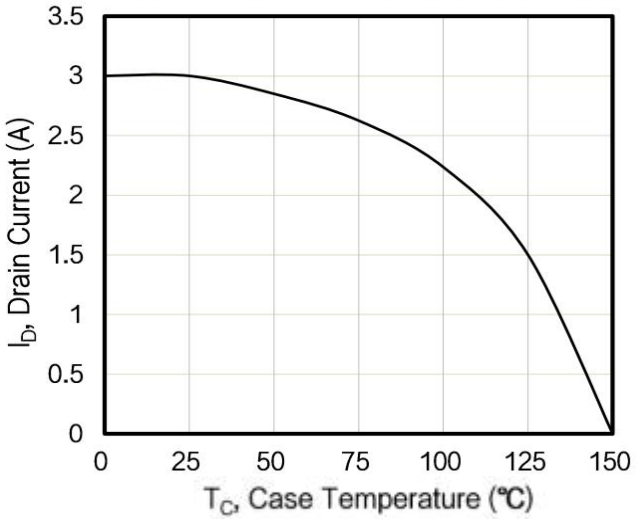



Figure 4.$BV_{DSS}$ Variation vs. Temperature

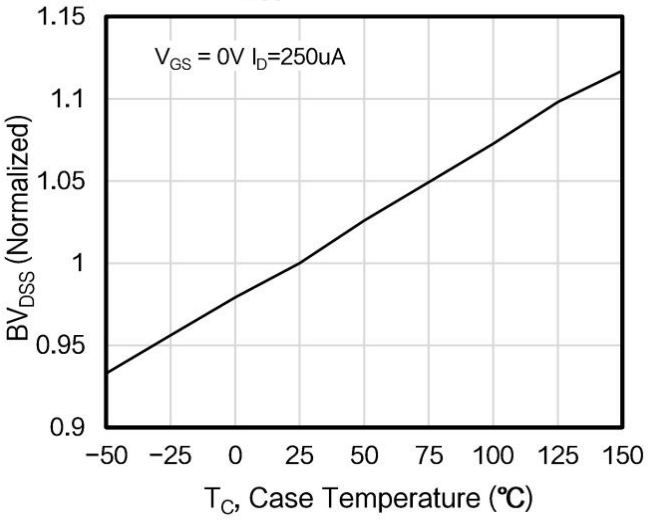



Figure 5. Transfer Characteristics

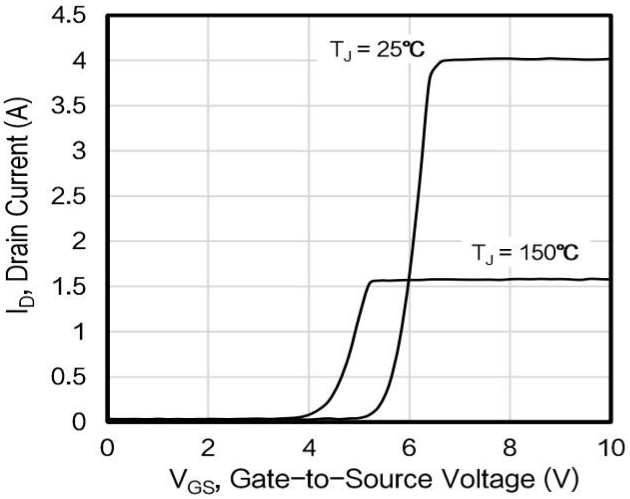
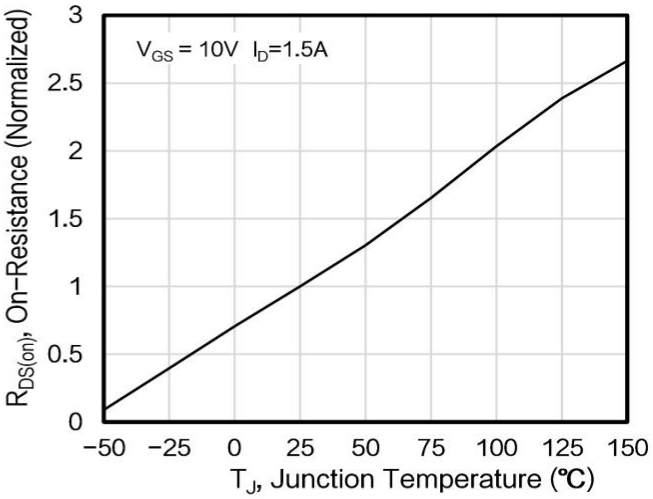



Figure 6. On-Resistance vs. Temperature





Copyright Reasunos

Figure 7. Capacitance

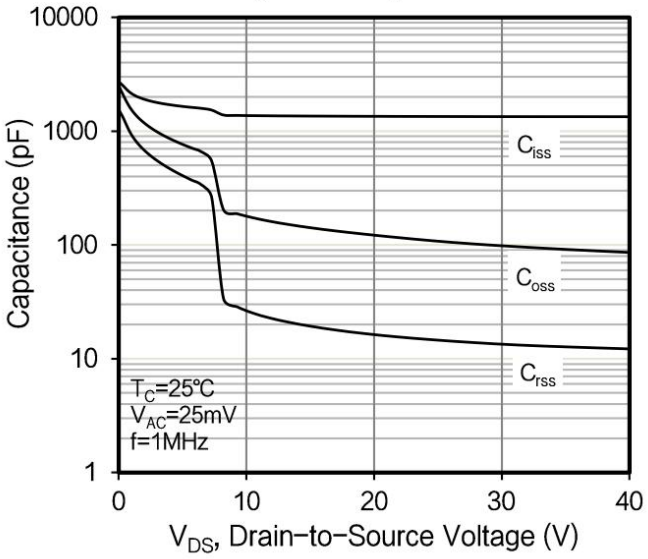



Figure 8. Gate Charge

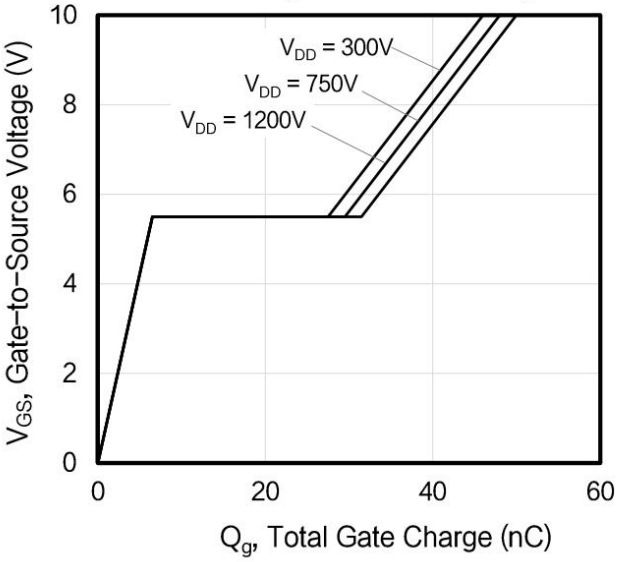
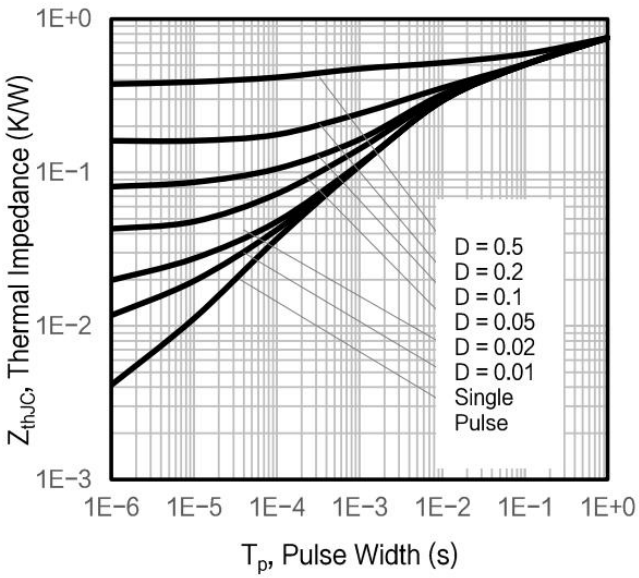



Figure 9. Transient Thermal Impedance





Copyright Reasunos

## Test Circuits and Waveforms

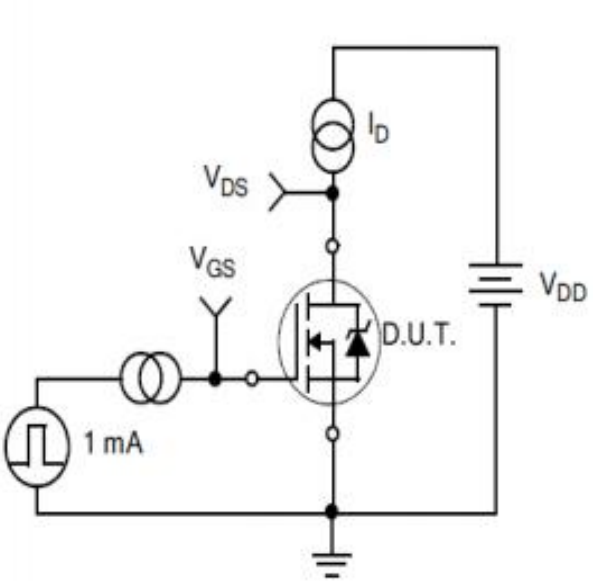



Figure10.
Gate Charge Test Circuit

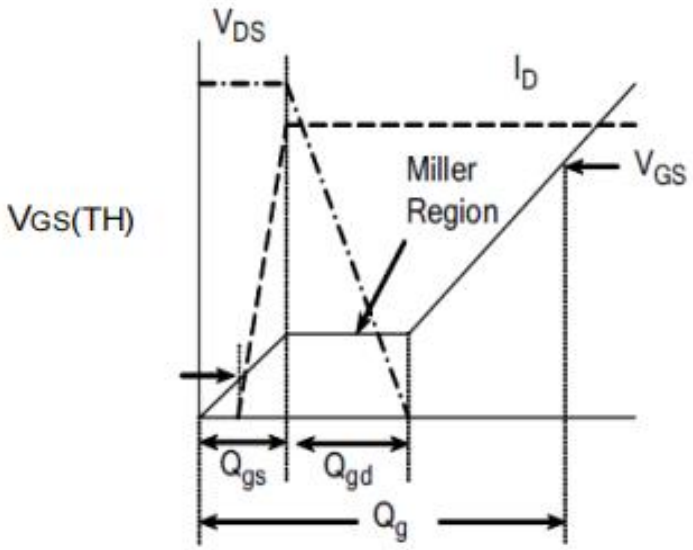



Figure11.
Gate Charge Waveform

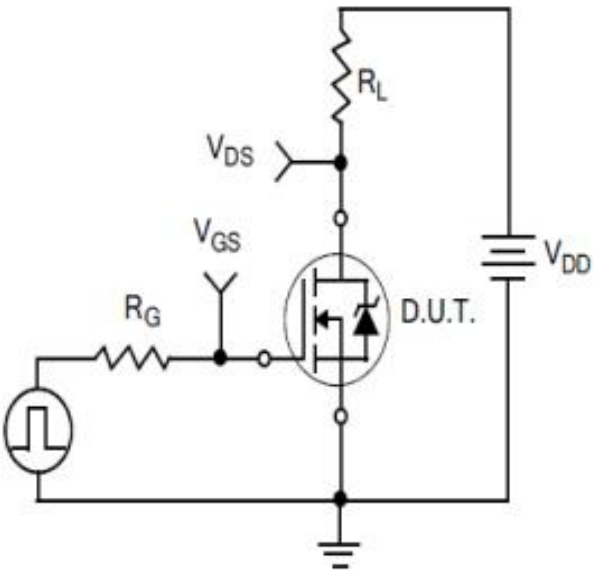



Figure12.
Resistive Switching Test Circuit

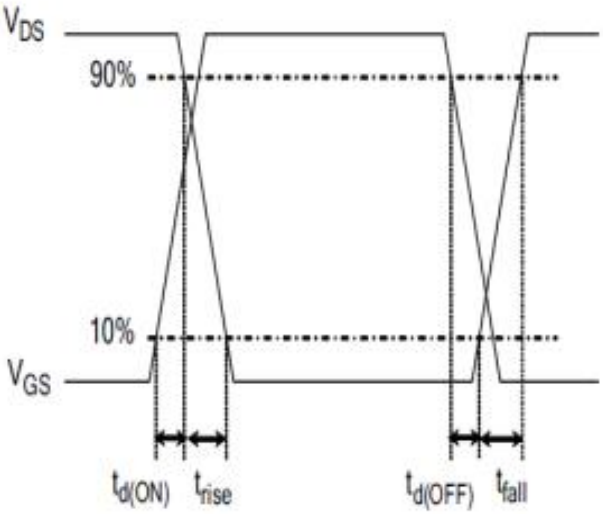



Figure13.
Resistive Switching Waveforms


Copyright Reasunos

## Test Circuits and Waveforms

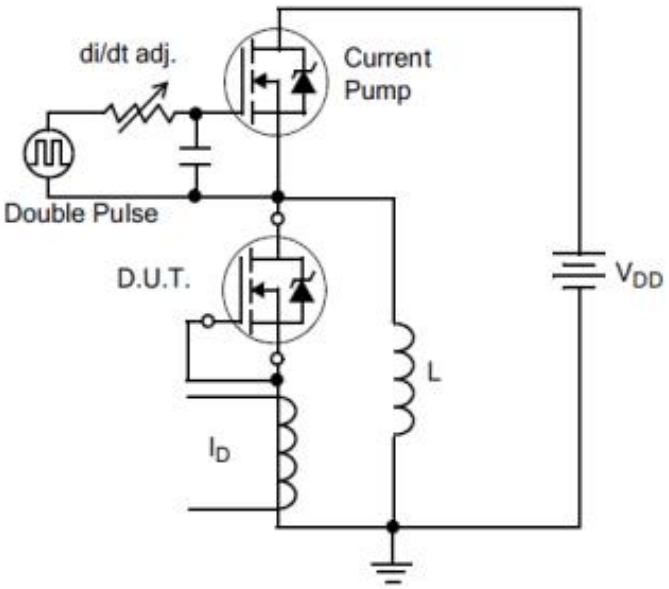



Figure14.Diode Reverse Recovery Test Circuit

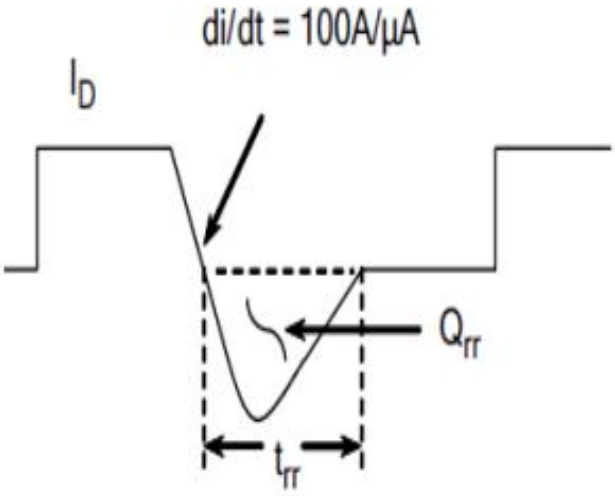



Figure15.Diode Reverse Recovery Waveform

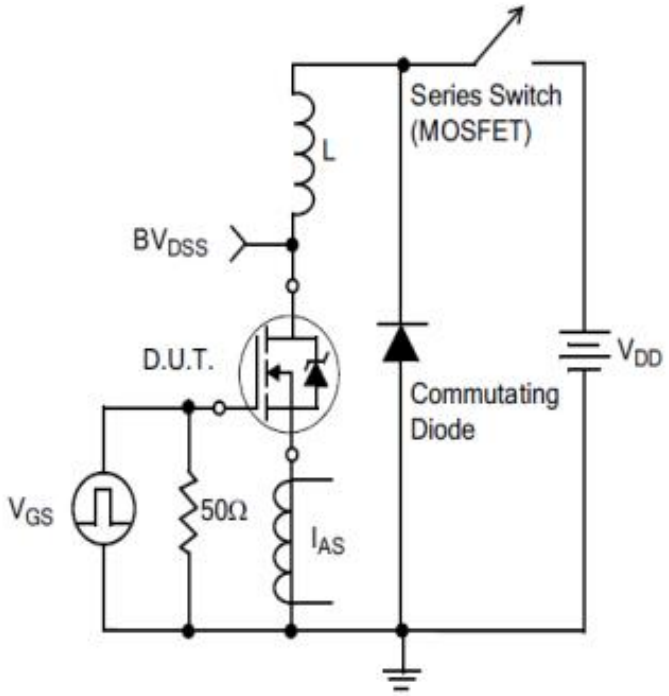
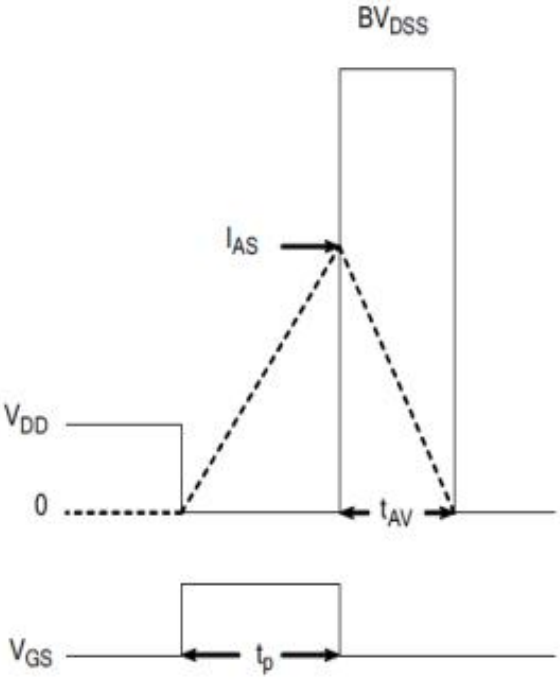



Figure16.Unclamped Inductive Switching Test Circuit

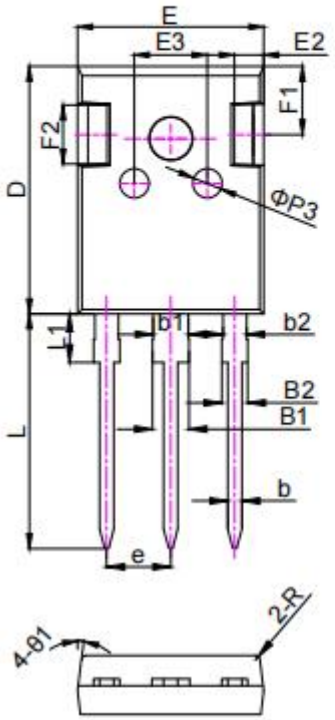


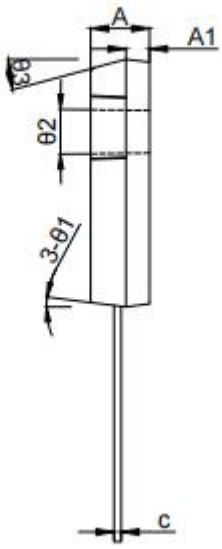

$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

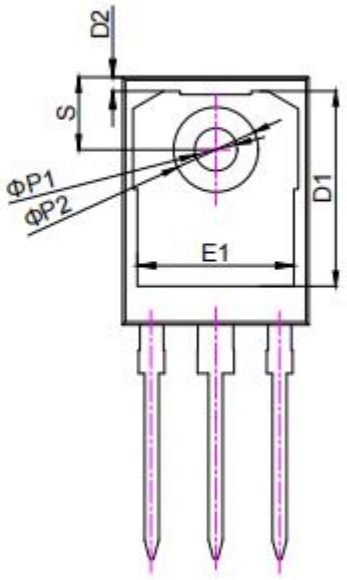
Figure17.Unclamped Inductive Switching Waveforms


Copyright Reasunos

## Package outline drawing(TO-247 Unit: mm )




| SYMBOL | MM | | | SYMBOL | MM | | |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | | MIN | NOM | MAX |
| *A | 4.80 | 5.00 | 5.20 | F1 | 5.70 | 5.80 | 5.90 |
| A1 | 1.90 | 2.00 | 2.10 | F2 | 4.85 | 5.00 | 5.15 |
| *b | 1.10 | 1.20 | 1.30 | *e | 5.39 | 5.44 | 5.49 |
| b1 | 2.90 | 3.00 | 3.10 | *L | 19.72 | 19.92 | 20.12 |
| b2 | 1.95 | 2.00 | 2.05 | *L1 | 4.03 | 4.13 | 4.23 |
| *B1 | 3.00 | 3.10 | 3.20 | θ1 | 5° | 7° | 9° |
| *B2 | 2.00 | 2.10 | 2.20 | θ2 | 1° | 2° | 3° |
| *c | 0.50 | 0.6 | 0.70 | θ3 | 13° | 15° | 17° |
| *D | 20.80 | 21 | 21.20 | *ΦP1 | 3.50 | 3.60 | 3.70 |
| D1 | 16.40 | 16.55 | 16.70 | ΦP2 | 7.09 | 7.19 | 7.29 |
| D2 | 1.07 | 1.17 | 1.27 | ΦP3 | 2.40 | 2.50 | 2.60 |
| *E | 15.60 | 15.80 | 16.00 | *Q1 | 2.31 | 2.41 | 2.51 |
| E1 | 13.11 | 13.26 | 13.41 | S | 6.05 | 6.15 | 6.25 |
| E2 | 2.40 | 2.50 | 2.60 | R | 0.30 | 0.40 | 0.50 |
| E3 | 6.10 | 6.20 | 6.30 | 带*为关键检验尺寸 | | | |

注:
1.表面粗糙度 Ra =1.14±0.20um
2. 带*为关键检验尺寸


Copyright Reasunos

## Disclaimers:

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights,nor the rights of others.Reproduction of inform- ation in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

## Life Support Policy:

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as cri- tical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.
As used herein:
1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.


Copyright Reasunos