

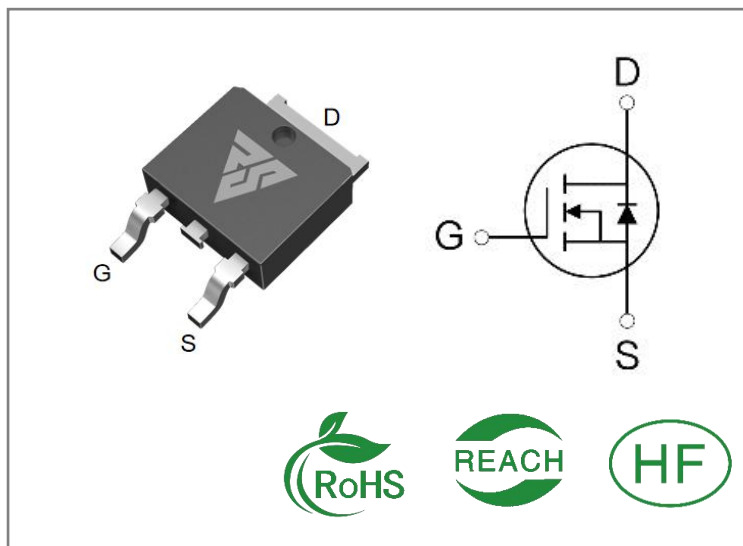
ID	$R_{DS(ON)}$ (Typ)	VDSS
5A	2.9Ω	500V

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply
- Power Factor Correction(PFC)

Features:

- Fast switching
- Integrate fast recovery diode
- 100% avalanche tested
- Improved dv/dt capability



Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSF5N50BD	T0-252	RSF5N50BD	Tape&reel	2500 PCS

Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	RSF5N50BD	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current $T_C=25^\circ\text{C}$	5	A
IDM	Pulsed Drain Current	12	A
PD	Power Dissipation	50	W
VGS	Gate- to- Source Voltage	± 30	V
EAR	Repetitive Avalanche Energy	0.35	mJ
EAS	Single Pulse Avalanche Energy $L=10\text{mH}, V_{DD}=50\text{V}, R_G=25\Omega, T_J=25^\circ\text{C}$	88.2	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	$^\circ\text{C}$
	Leads at 0.063in(1.6mm)from Case for 10 seconds		
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RSF5N50BD	Units	Test Conditions
R θ JC	Junction-to-Case	2.5	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 150 $^{\circ}\text{C}$
R θ JA	Junction-to-Ambient	100		1 cubic foot chamber, free air.

OFF Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500	--	--	V	VGS=0V ID=250 μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=500V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	2.9	3.5	Ω	VGS=10V ID=1.5A
VGS (TH)	Gate Threshold Voltage	3.0	--	4.0	V	VGS=VDS ID=250 μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	33	--	nS	VDS=250V ID=3A RG=25 Ω
trise	Rise Time	--	5	--		
td(OFF)	Turn- OFF Delay Time	--	50	--		
tfall	Fall Time	--	18	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	310	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	39	--		
Crss	Reverse Transfer Capacitance	--	12	--		
RG	Internal Gate Resistance	--	3.5	--	Ω	
Qg	Total Gate Charge	--	8	--	nC	VDS=400V ID=3A VGS=10V
Qgs	Gate- to- Source Charge	--	1.2	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	5	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	5	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	12	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=1.5A VGS=0V
trr	Reverse Recovery Time	--	90	--	nS	VR=250V IS=3A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	0.13	--	nC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

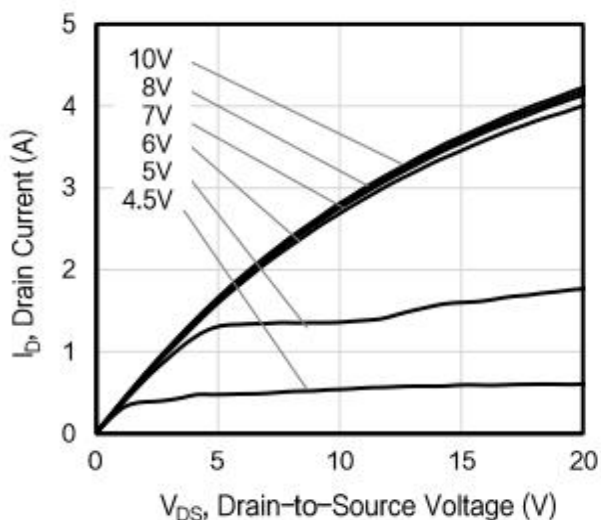


Figure 2. Body Diode Forward Voltage

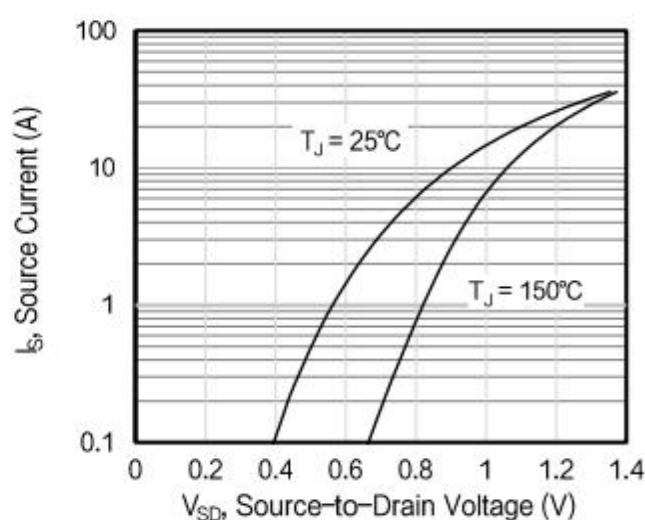


Figure 3. Drain Current vs. Temperature

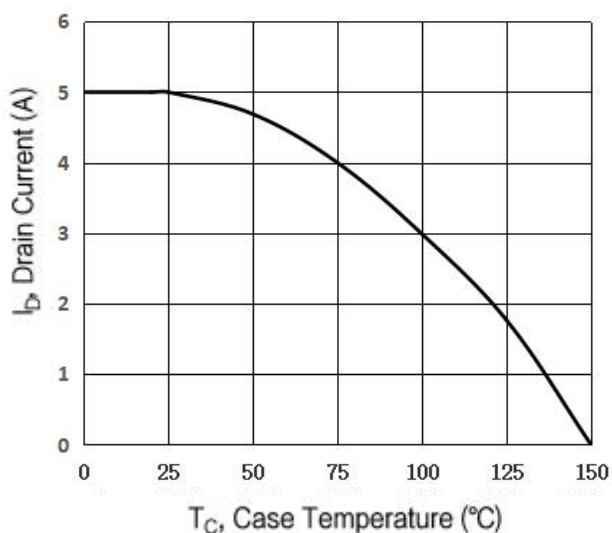


Figure 4. BV_{DSS} Variation vs. Temperature

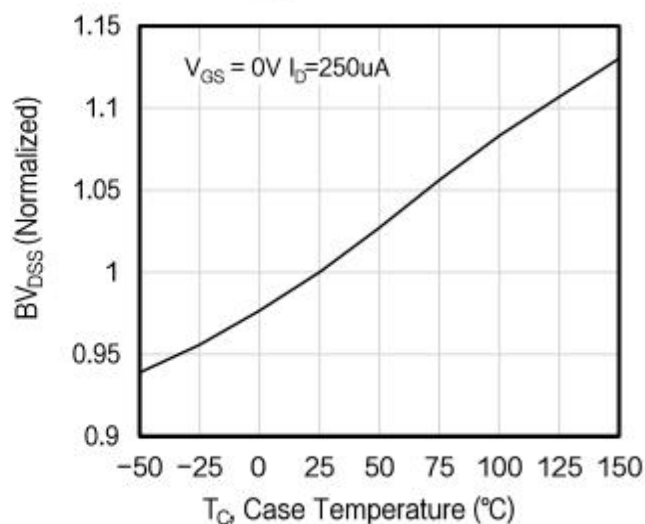


Figure 5. Transfer Characteristics

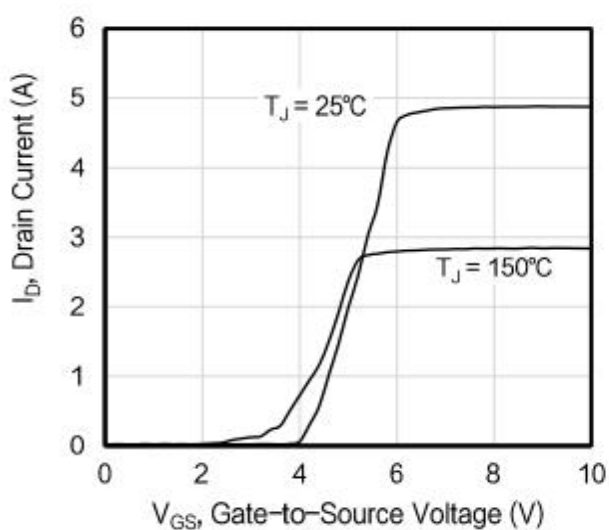


Figure 6. On-Resistance vs. Temperature

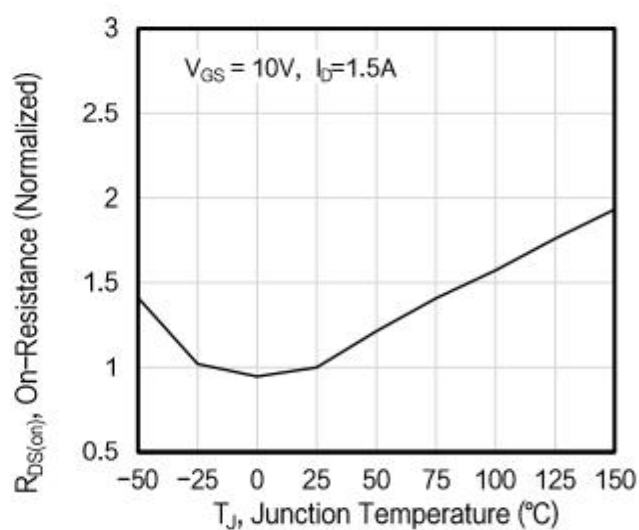


Figure 7. Capacitance

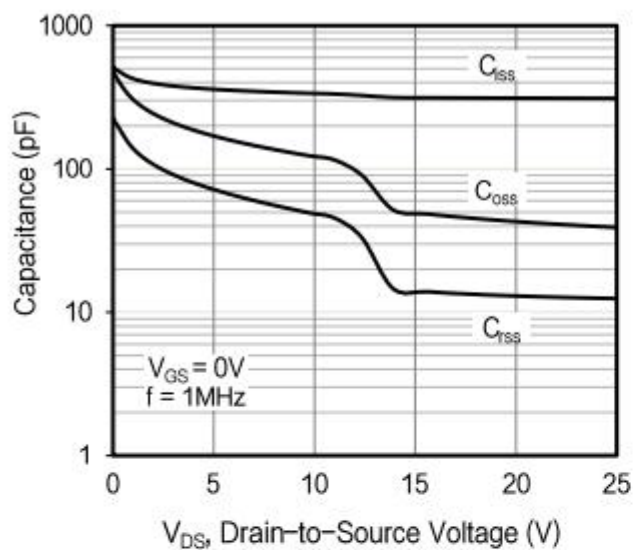


Figure 8. Gate Charge

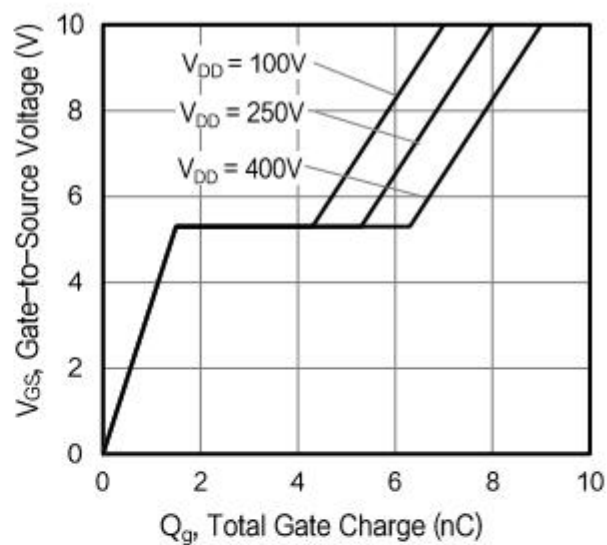
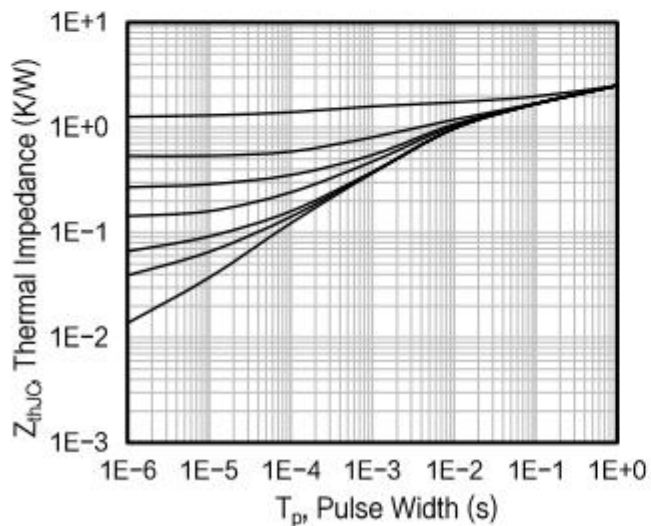


Figure 9. Transient Thermal Impedance



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

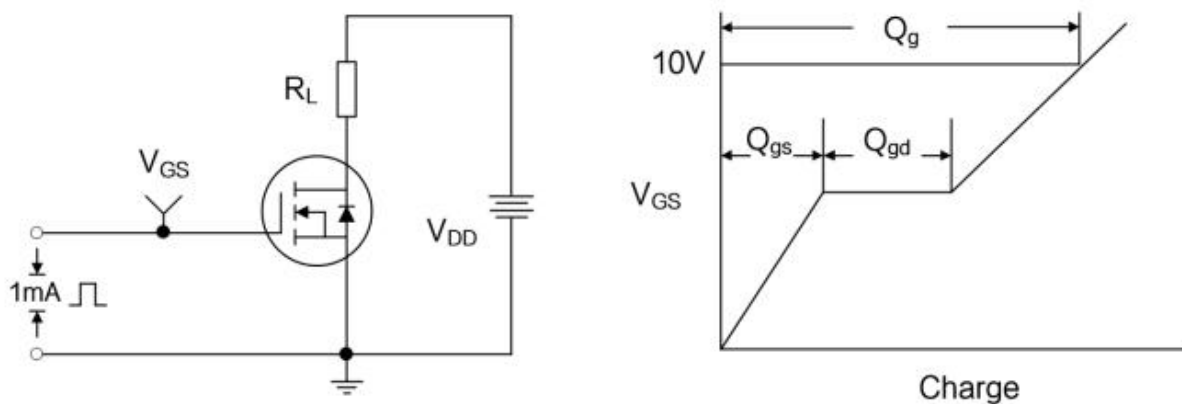


Figure B: Resistive Switching Test Circuit and Waveform

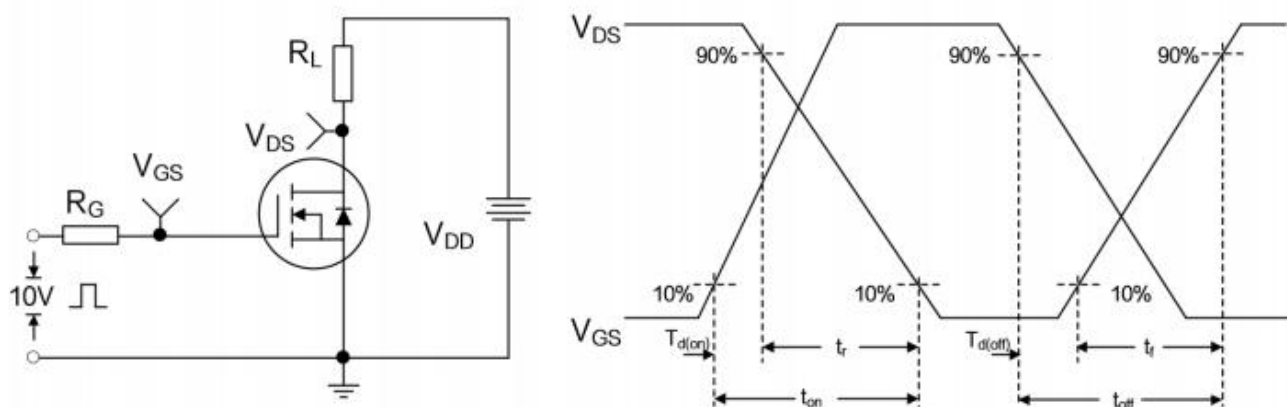
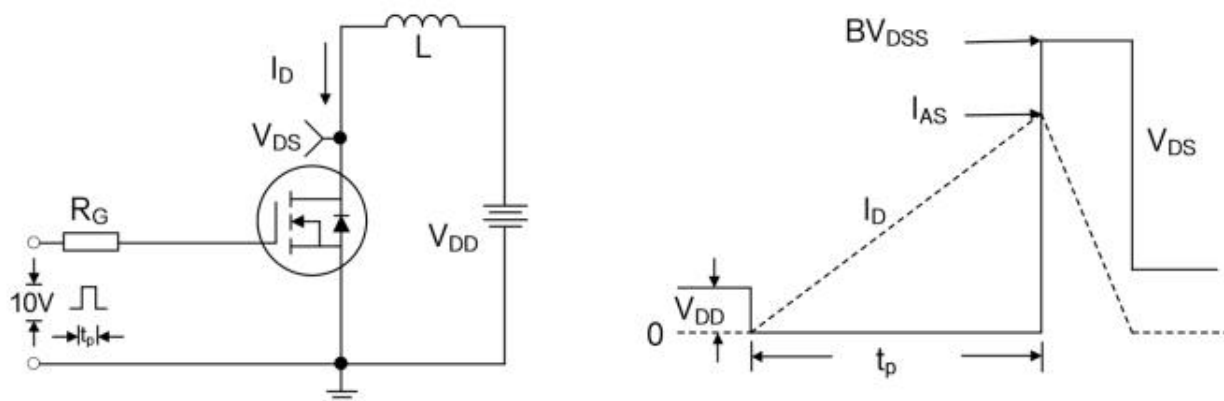
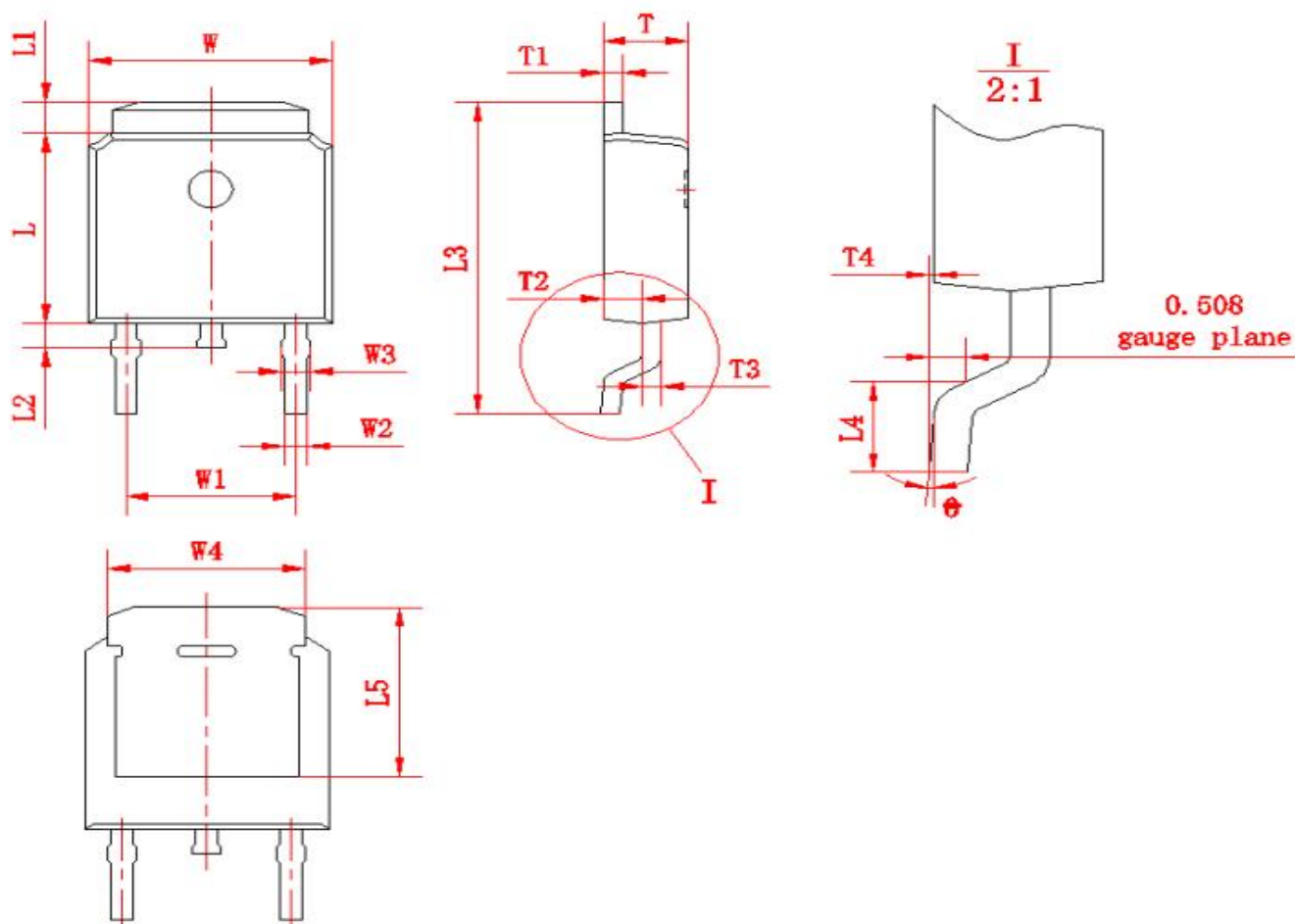


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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