

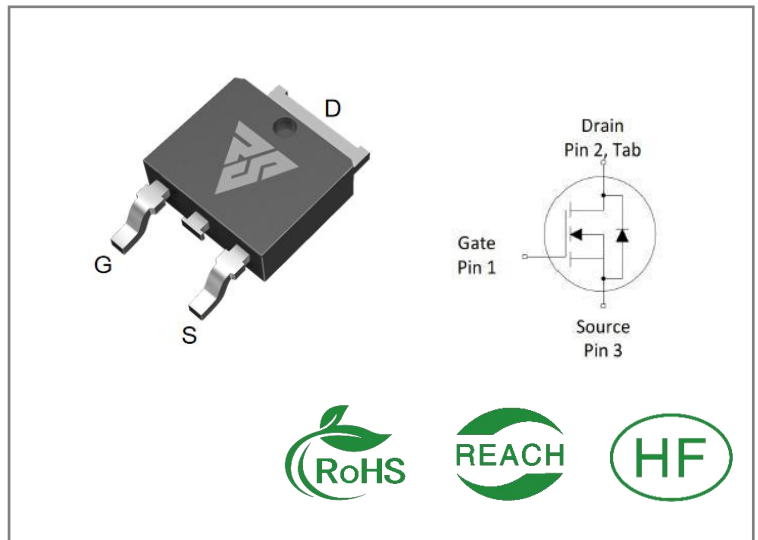
ID	R _{DS(ON)} (Typ)	VDSS
4A	2.3Ω	650V

Applications:

- LED power supplies
- Cell Phone Charger
- Standby Power

Features:

- Low gate charge
- Low Ciss
- Fast switching



Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS4N65BD	T0-252	RS4N65BD	Tape&reel	2500 PCS

Absolute Maximum Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS4N65BD	Units
VDSS	Drain-to-Source Voltage	650	V
ID	Continuous Drain Current TC=25°C(Note*1)	4	A
IDM	Pulsed Drain Current (Note*2)	16	
PD	Power Dissipation TC=25°C	74	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy L = 10mH, VD=50V, TC=25°C	180	mJ
TL TPKG	Maximum Temperature for Soldering	300	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS4N65BD	Units	Test Conditions
R θ JC	Junction-to-Case	1.69	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\text{C}$
R θ JA	Junction-to-Ambient	54		1 cubic foot chamber, free air.

OFF Characteristics TJ= 25 $^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650	--	--	V	VGS=0V ID=250 μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=650V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics TJ=25 $^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	2.3	2.6	Ω	VGS=10V ID=2A
VGS(TH)	Gate Threshold Voltage	2.0	2.9	4.0	V	VGS=VDS ID=250 μA
Rg	Gate Resistance	--	3.9	--	Ω	VGS=0V VDS=0V f=1MHz
Gfs	Forward Transconductance	--	3	--	S	VDS=10V ID=2A

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	6	--	nS	VDS=325V ID=4A RG=10 Ω VGS=10V
trise	Rise Time	--	11	--		
td(OFF)	Turn- OFF Delay Time	--	14	--		
tfall	Fall Time	--	41	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	587	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	48	--		
Crss	Reverse Transfer Capacitance	--	3	--		
Qg	Total Gate Charge	--	16	--	nC	VDS=520V ID=4A VGS=10V
Qgs	Gate- to- Source Charge	--	4	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	3	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	4	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	16	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=4A VGS=0V
trr	Reverse Recovery Time	--	375	--	nS	VGS=0V VDS=30V IS=1A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	533	--	μC	

Notes:

* 1. Limited by TJ MAX<150°C, Maximum Duty Cycle D=0.5, TO-220 equivalent.

* 2. This single-pulse measurement was taken under Tj_Max = 150°C.

Typical Feature Curve

Figure.1 Output Characteristics $T_J = 25^\circ\text{C}$

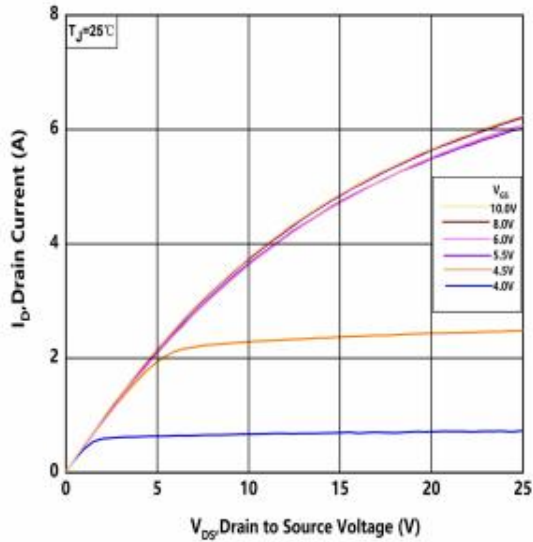


Figure.2 Transfer Characteristic for Various Junction Temperatures

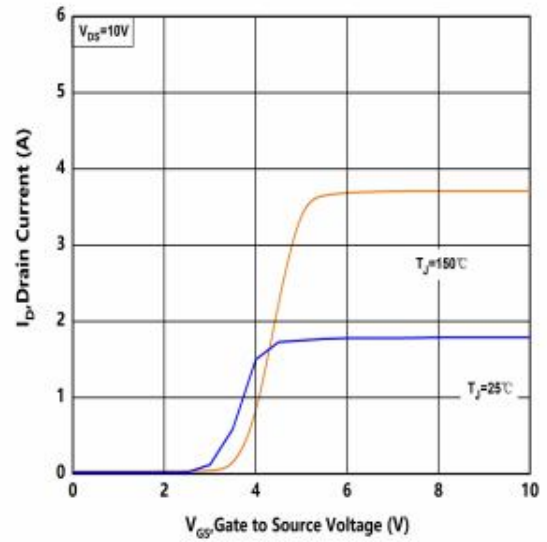


Figure.3 On-Resistance vs Drain Current For Various Gate Voltage

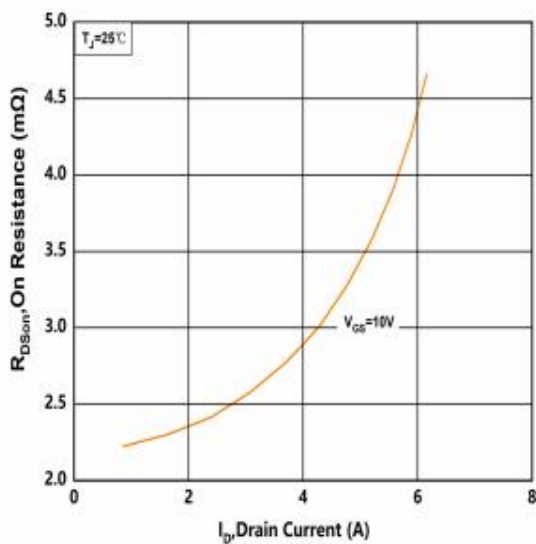
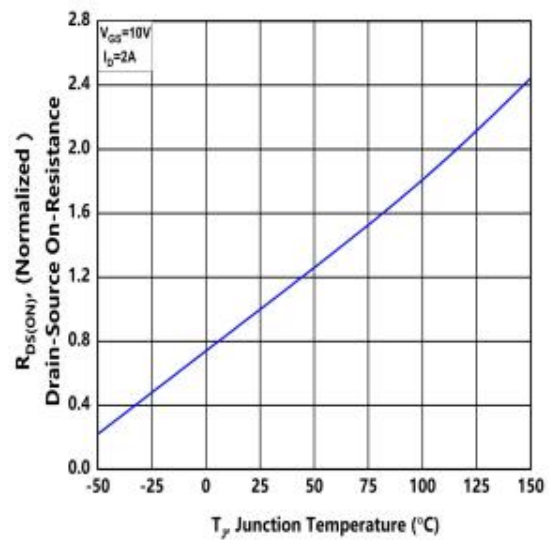


Figure.4 Typical On-Resistance vs Junction Temperature



Typical Feature Curve

Figure.5 Typical Threshold Voltage vs Junction Temperature

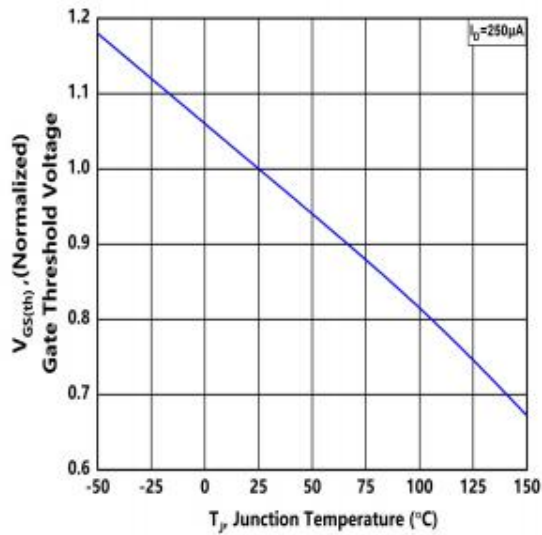


Figure.6 Typical Breakdown Voltage vs Junction Temperature

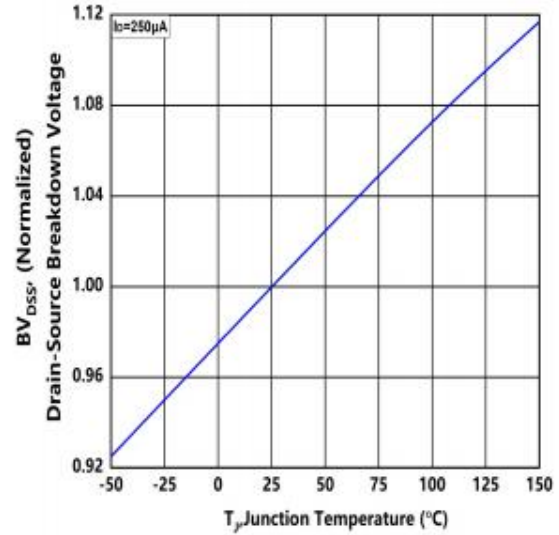


Figure.7 Typical Capacitance vs Drain to Source Voltage

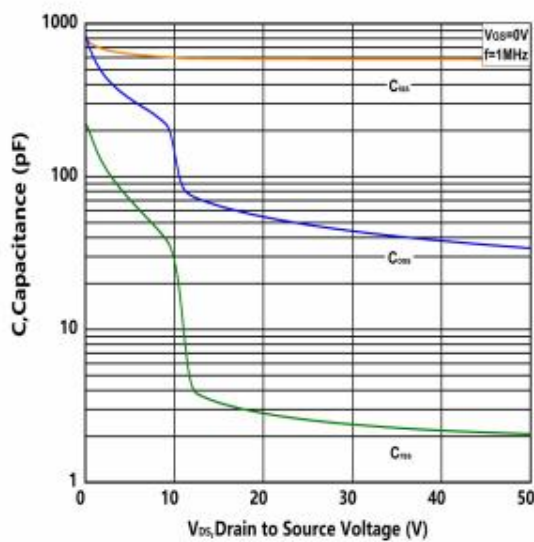


Figure.8 Typical Gate Charge vs Gate to Source Voltage

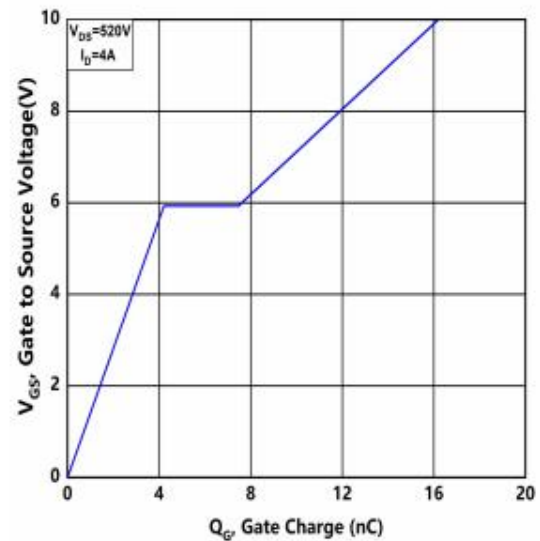


Figure.9 Typical Body Diode Characteristics

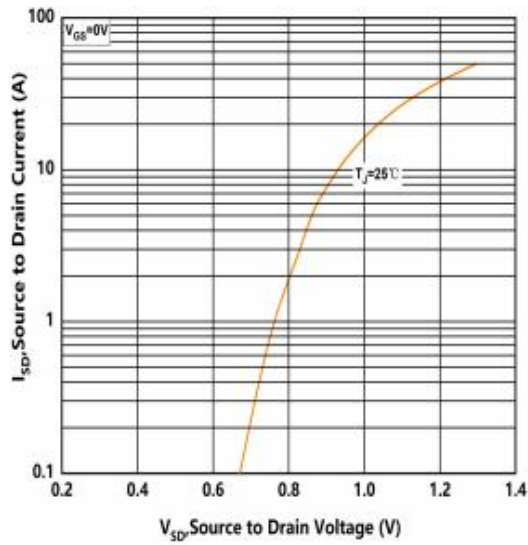


Figure.10 Maximum power Dissipation Derating vs Case Temperature

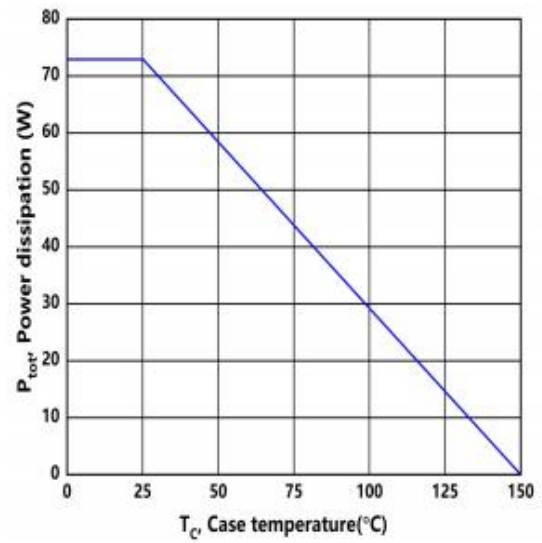


Figure.11 Safe Operating Area

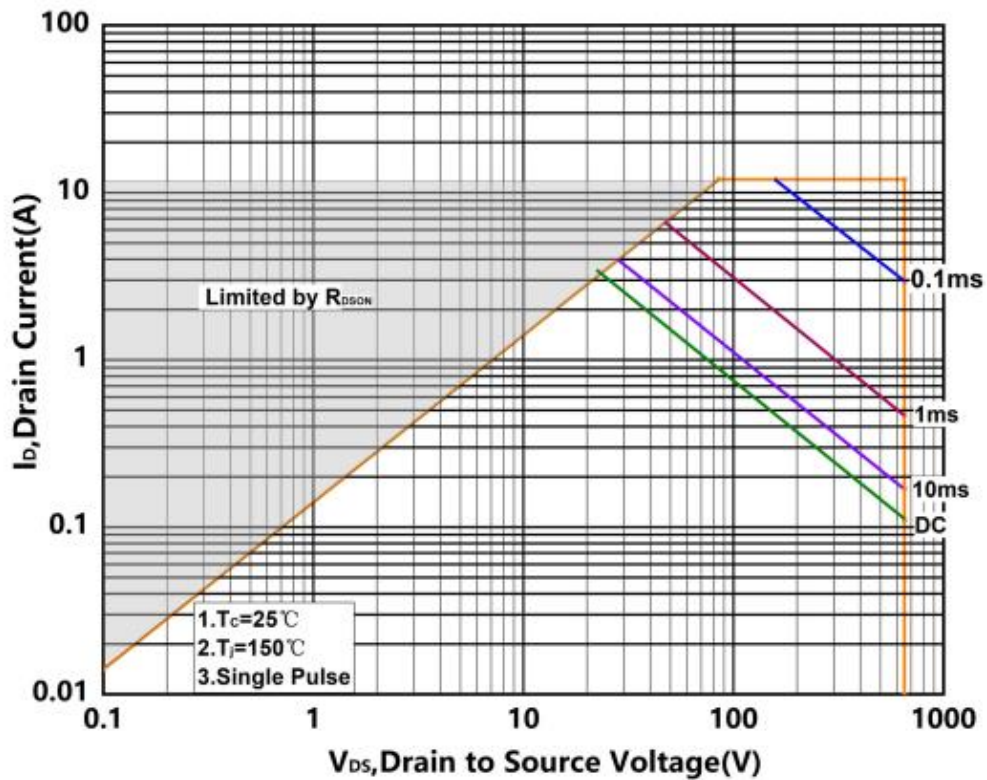
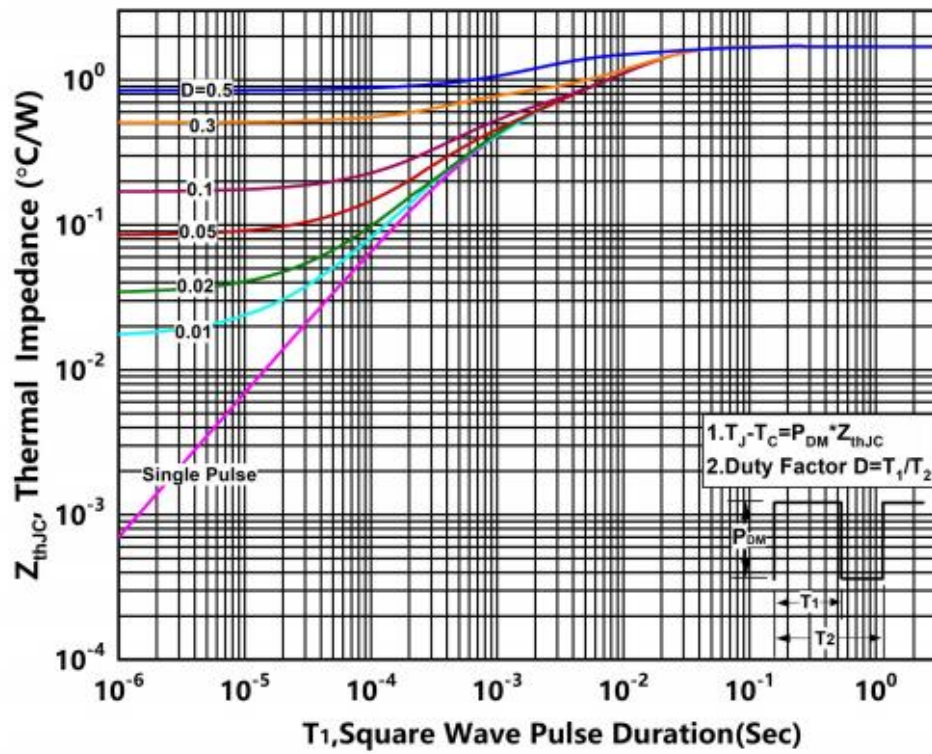
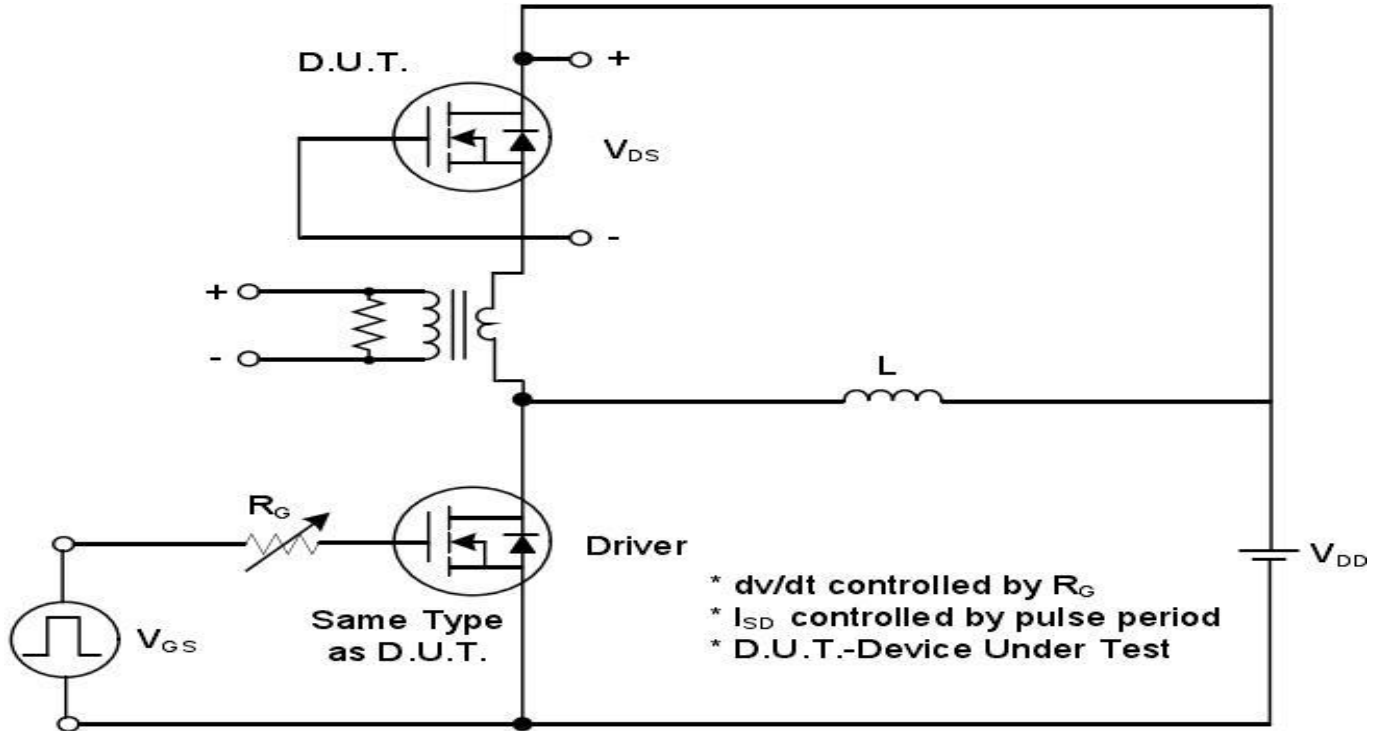


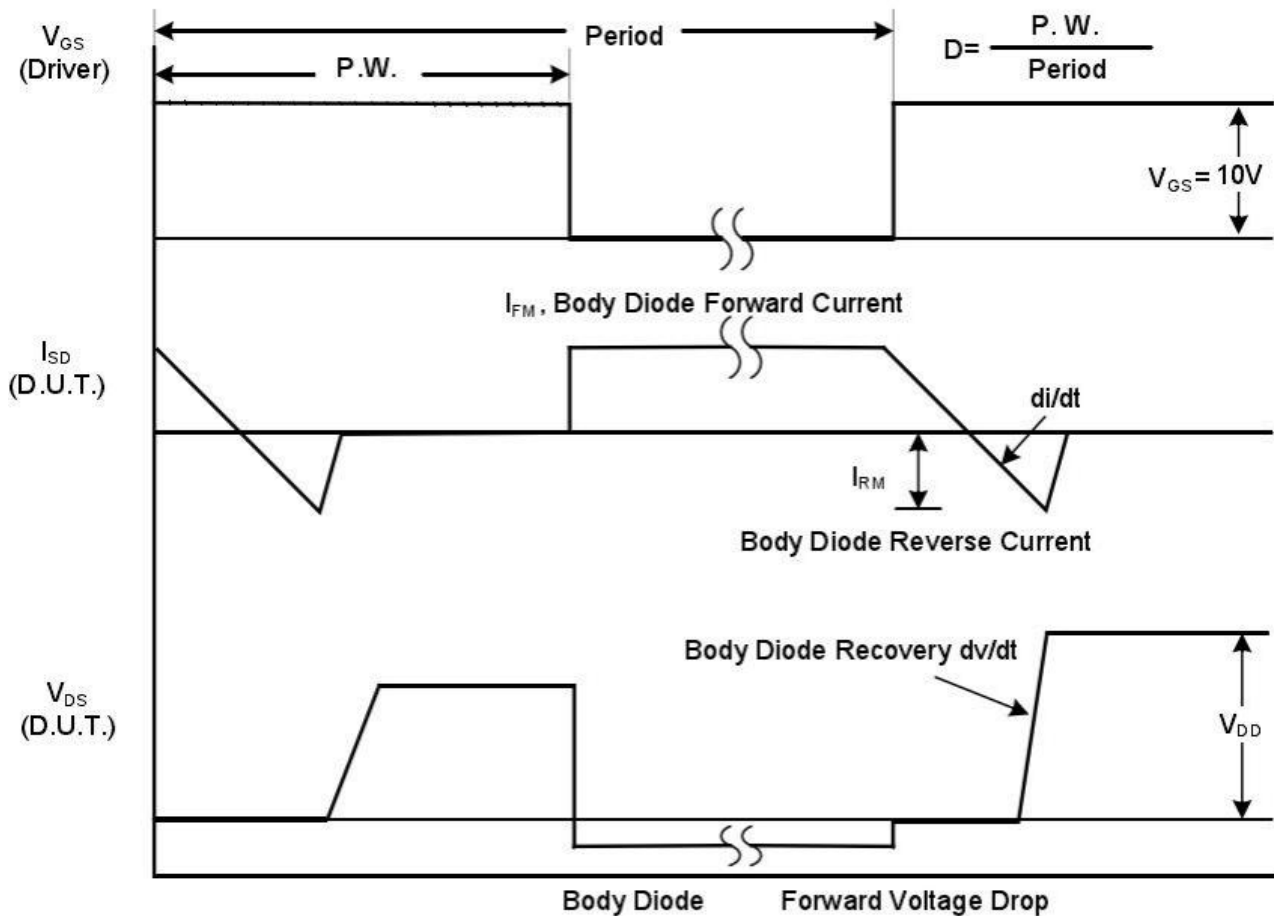
Figure.12 Transient Thermal Impedance (Junction - Case)



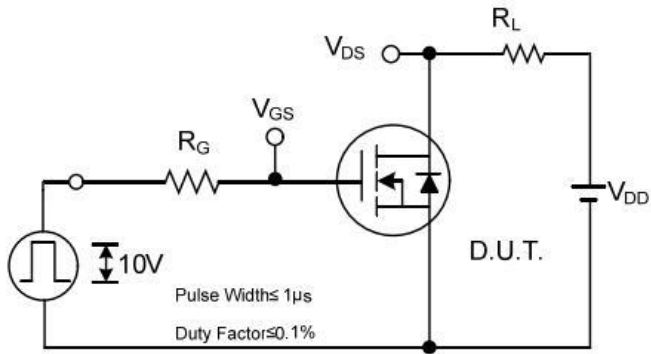
Test Circuits and Waveforms



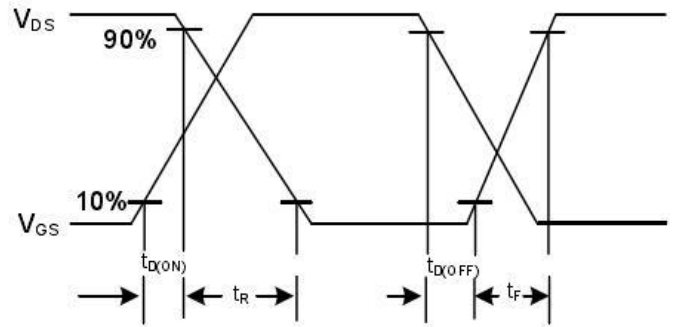
Peak Diode Recovery dv/dt Test Circuit



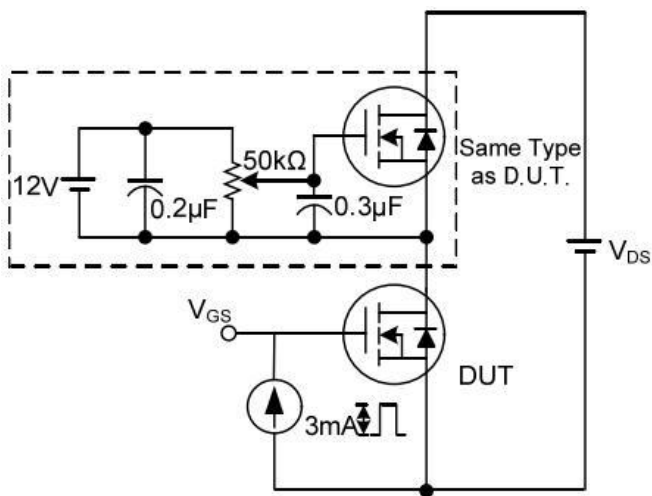
Peak Diode Recovery dv/dt Waveforms



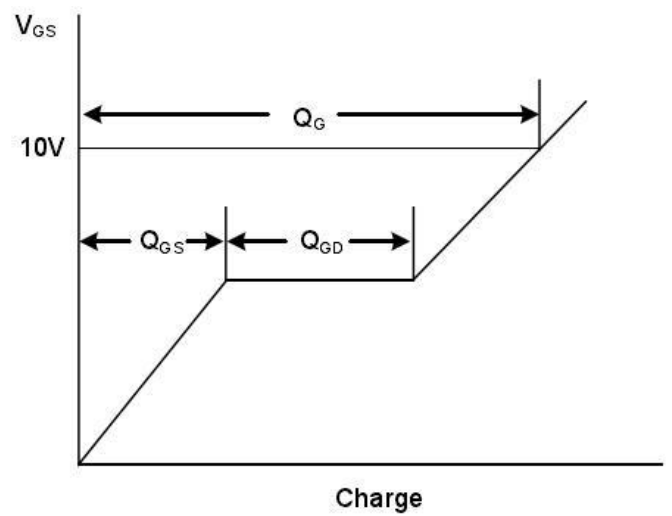
Switching Test Circuit



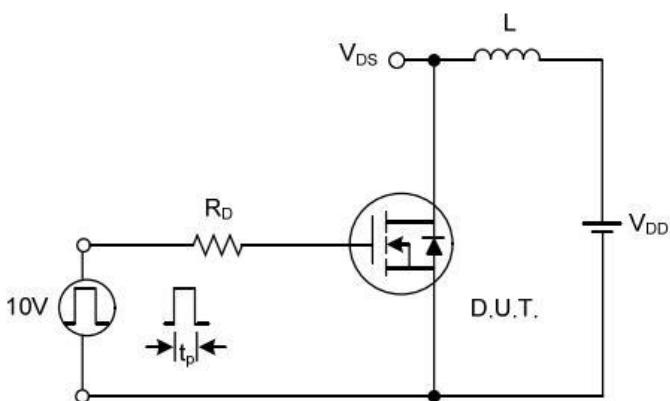
Switching Waveforms



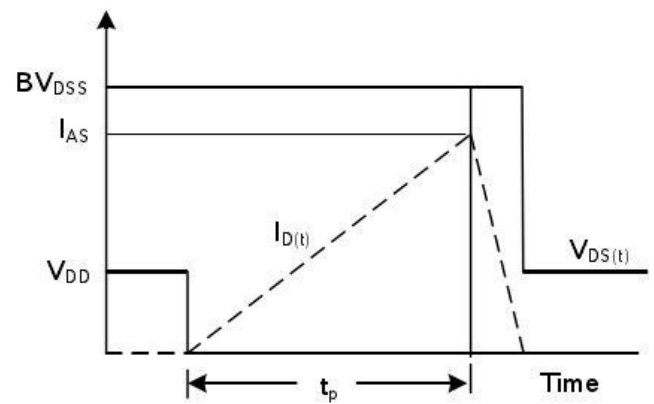
Gate Charge Test Circuit



Gate Charge Waveform

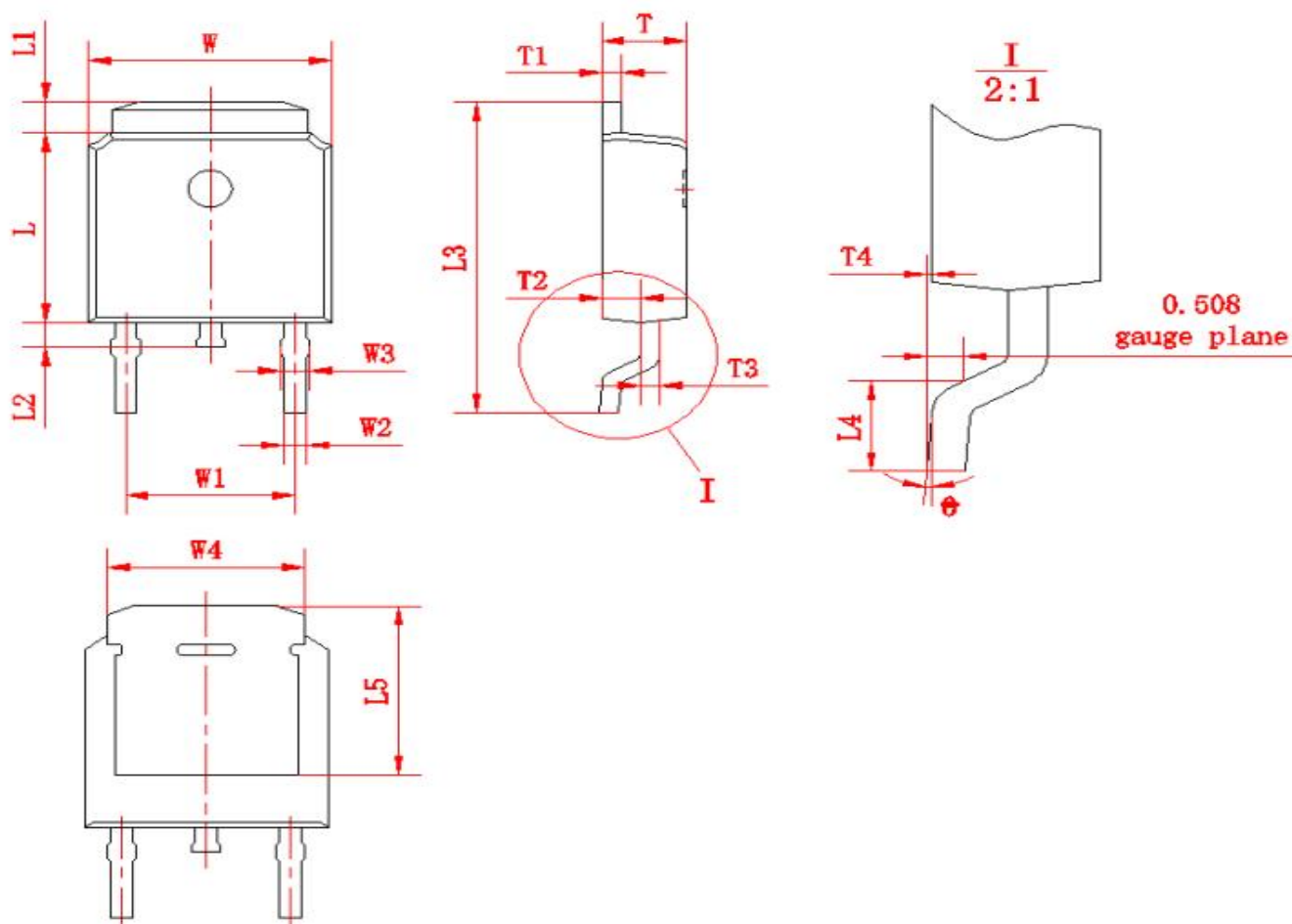


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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