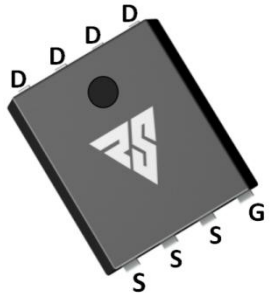
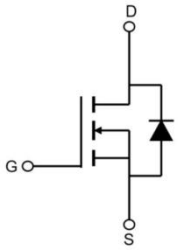
ID	R_{DS}(ON)(Typ)	VDSS
210A	1.5mΩ	40V





Applications:
- Power switching application
- Uninterruptible power supply
- DC-DC convertor

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS40N210G	PDFN5*6	RS40N210G	Tape&reel	5000 PCS

Absolute Maximun Ratings Tc= 25℃ unless otherwise specified

Symbol	Parameter	RS40N210G	Units
VDSS	Drain-to-Source Voltage	40	V
ID	Continuous Drain Current TC=25℃	210	A
ID	Continuous Drain Current TC=100℃	137	
IDM	Pulsed Drain Current	840	
PD	Power Dissipation	120	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH，RG = 25 Ω,TJ=25℃，VGS=35V，IAS=41A	420	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS40N210G	Units	Test Conditions
RθJC	Junction-to-Case	1.0	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	40	--	--	V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=40V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	1.5	1.9	mΩ	VGS=10V ID=30A
VGS(TH)	Gate Threshold Voltage	1.0	1.7	2.5	V	VGS=VDS ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	13	--	nS	VDS=20V RG=3Ω VGS=10V ID=30A
trise	Rise Time	--	9	--		
td(OFF)	Turn- OFF Delay Time	--	101	--		
tfall	Fall Time	--	15	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	14705	--	pF	VGS=0V VDS=20V f=1MHz
Coss	Output Capacitance	--	846	--		
Crss	Reverse Transfer Capacitance	--	829	--		
Qg	Total Gate Charge	--	95	--	nC	VDS=20V ID=30A VGS=10V f=1MHz
Qgs	Gate- to- Source Charge	--	15	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	19	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	210	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	840	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=30A VGS=0V
trr	Reverse Recovery Time	--	35	--	nS	IS=30A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	24.2	--	nC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 0.5%

Typical Feature Curve

Figure1: Output Characteristics

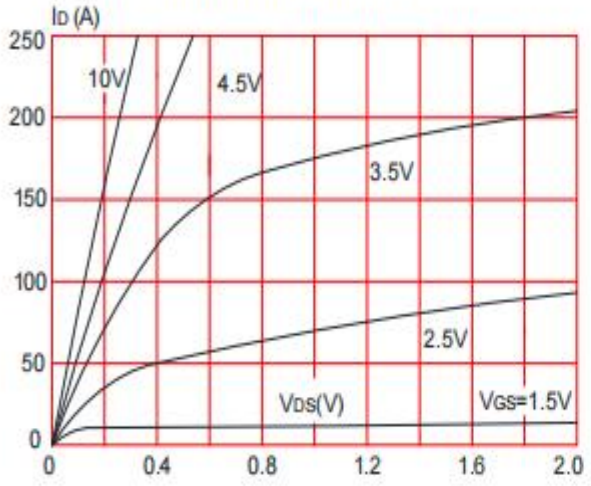


Figure 2: Typical Transfer Characteristics

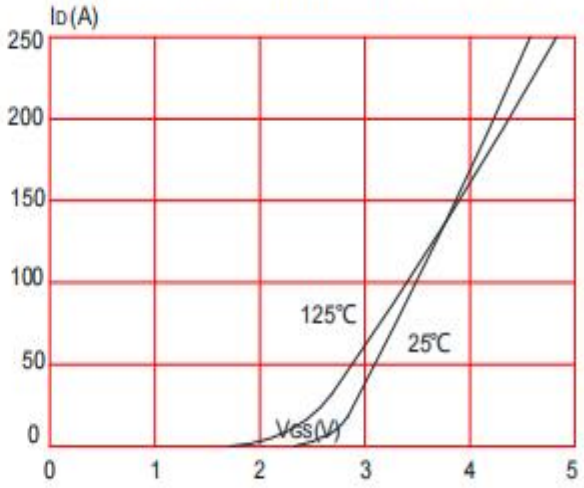


Figure 3: On-resistance vs. Drain Current

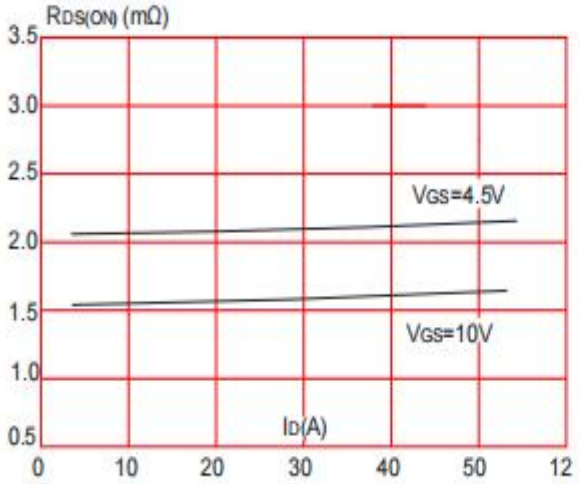


Figure 4: Body Diode Characteristics

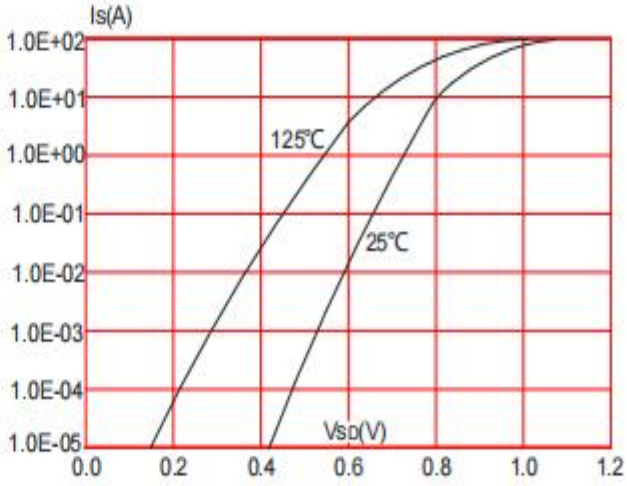


Figure 5: Gate Charge Characteristics

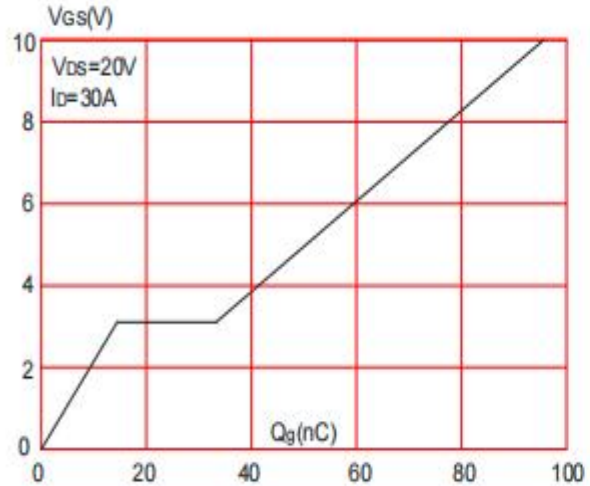


Figure 6: Capacitance Characteristics

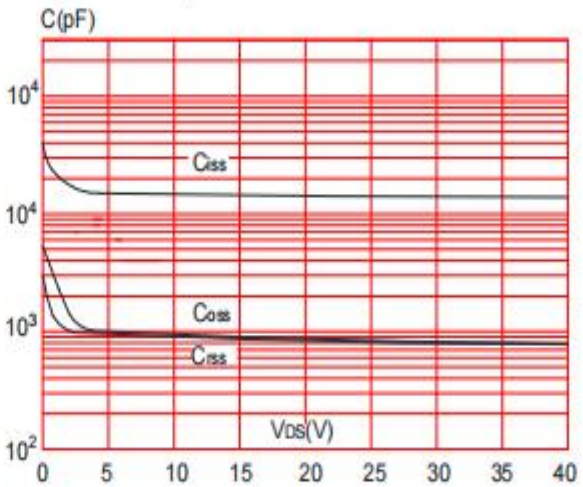


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

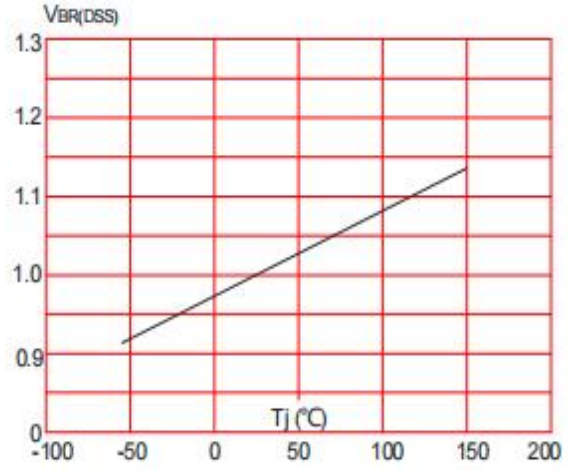


Figure 8: Normalized on Resistance vs. Junction Temperature

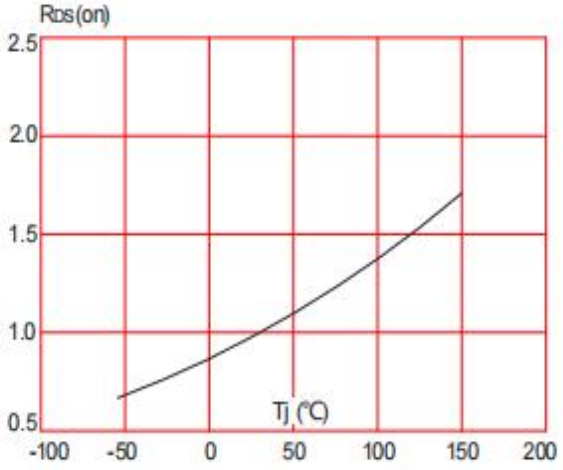


Figure 9: Maximum Safe Operating Area

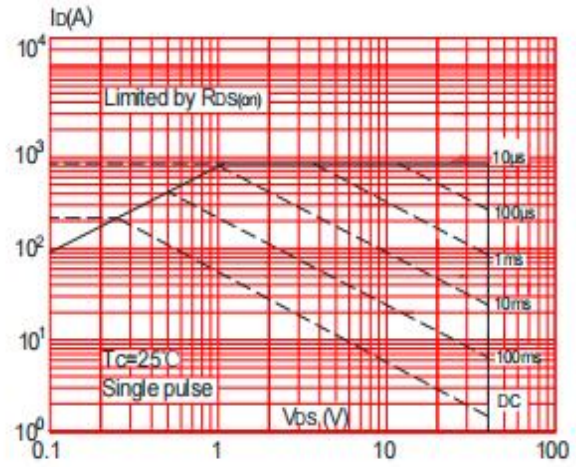


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

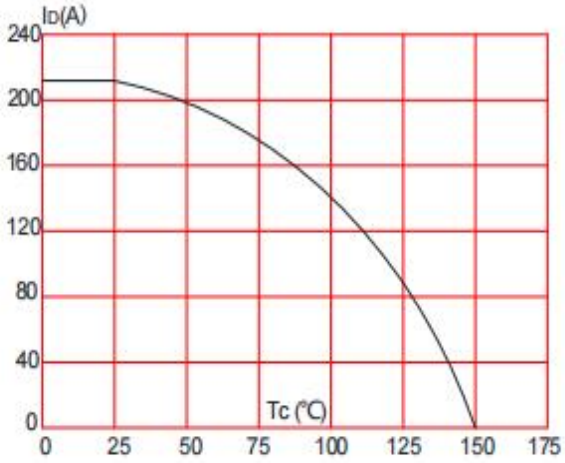
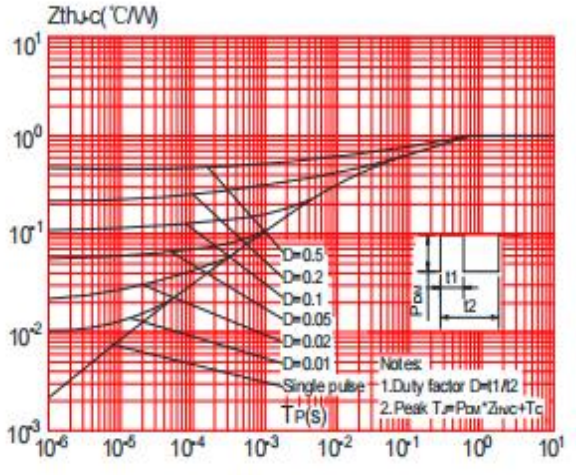


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test ircuits and Waveforms

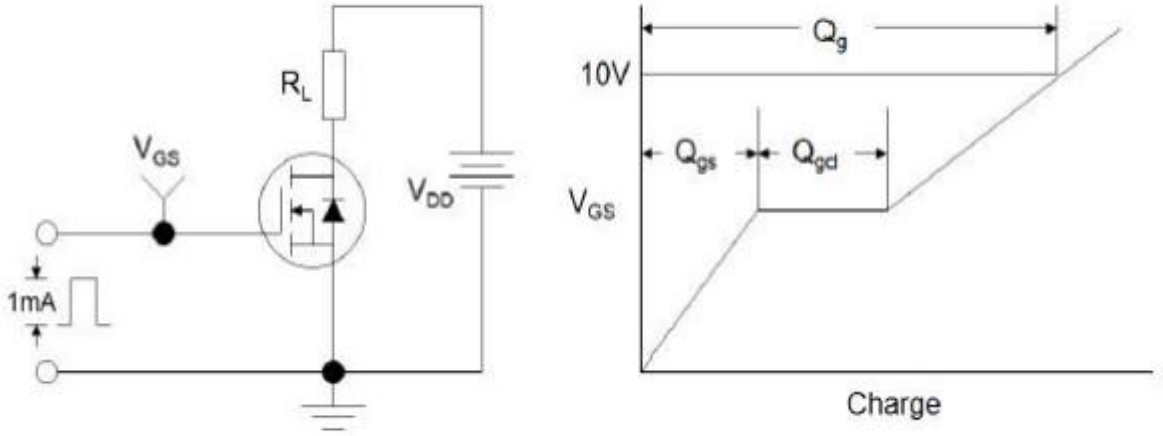


Figure1:Gate Charge Test Circuit & Waveform

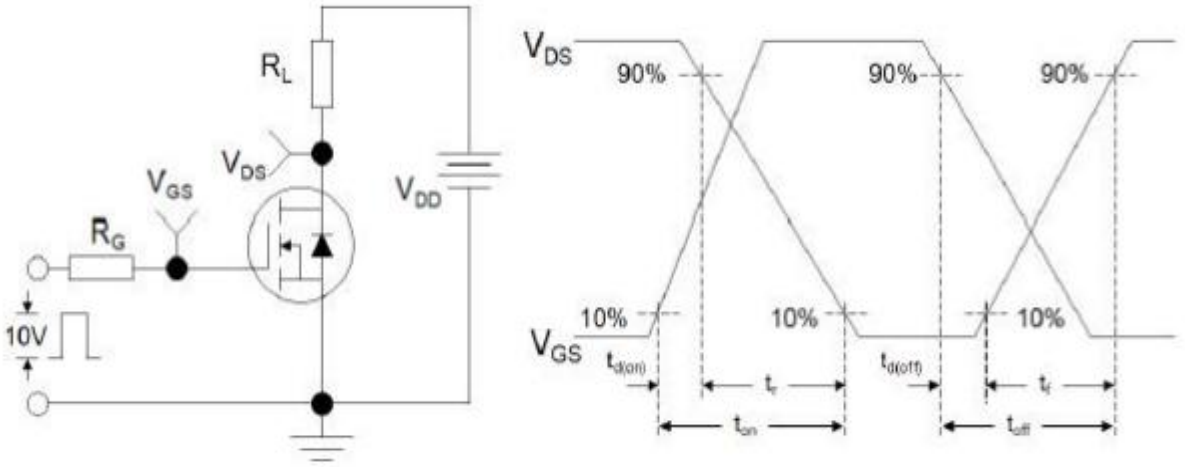


Figure 2: Resistive Switching Test Circuit & Waveforms

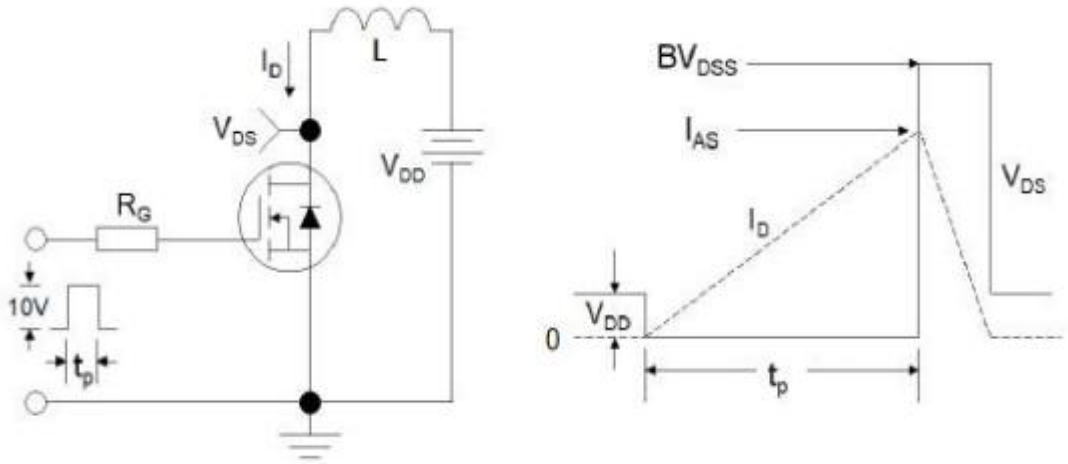
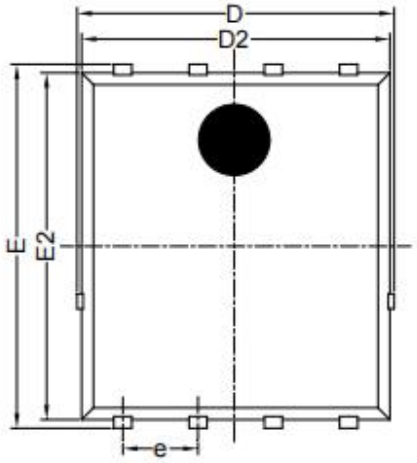
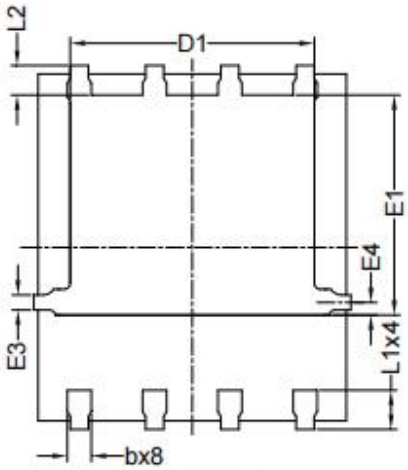


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

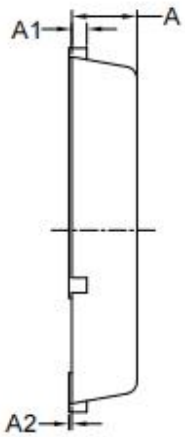
Package outline drawing(DFN5*6 Unit: mm)



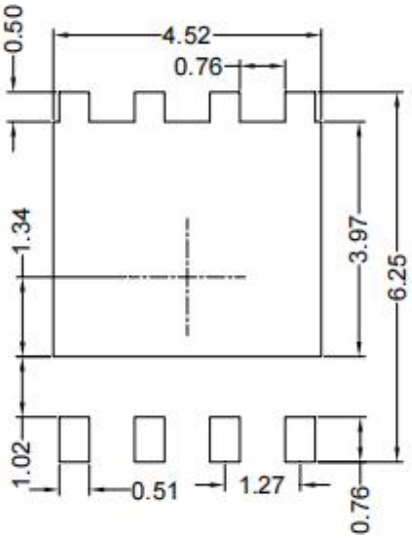
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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