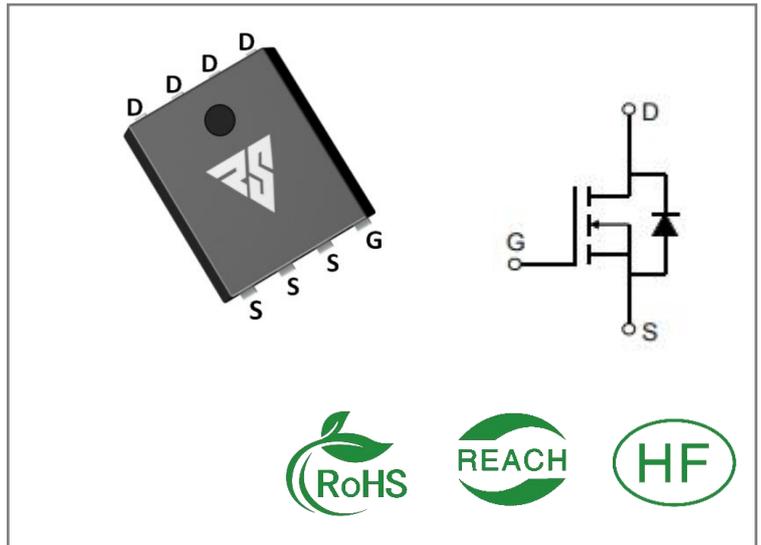


ID	R _{DS(ON)} (Typ)	VDSS
92A	6.0mΩ	100V


Applications:

- Load Switch
- PWM Applications
- Power Management

Features:

- Advanced Split Gate Trench Technology
- Excellent RDS (ON) and Low Gate Charge

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS100N100UG	PDFN5*6	RS100N100UG	Tape&reel	5000 PCS

Absolute Maximun Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS100N100UG	Units
VDSS	Drain-to-Source Voltage	100	V
ID	Continuous Drain Current TC=25°C	92	A
ID	Continuous Drain Current TC=100°C	55	
IDM	Pulsed Drain Current (Note*1)	368	
PD	Power Dissipation	125	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy,TJ=25°C L = 0.5mH, VDD=50V, VG=10V, RG = 25 Ω,IAS=23A	132	mJ
TL TPKG	Maximum Temperature for Soldering	300	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS100N100UG	Units	Test Conditions
R θ JC	Junction-to-Case	1	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 °C

OFF Characteristics TJ= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	100	--	--	V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=100V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	6.0	7.8	mΩ	VGS=10V ID=30A
		--	8.0	10.0		VGS=4.5V ID=20A
VGS(TH)	Gate Threshold Voltage	1.4	2.0	2.6	V	VGS=VDS ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	12	--	nS	VDS=50V RG=3Ω VGS=10V ID=20A
trise	Rise Time	--	15	--		
td(OFF)	Turn- OFF Delay Time	--	33	--		
tfall	Fall Time	--	20	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	2370	--	pF	VGS=0V VDS=50V f=1MHz
Coss	Output Capacitance	--	910	--		
Crss	Reverse Transfer Capacitance	--	14	--		
Qg	Total Gate Charge	--	45	--	nC	VDS=50V ID=20A VGS=0 to10V
Qgs	Gate- to- Source Charge	--	9	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	7	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	92	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	368	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=30A,VGS=0V
trr	Reverse Recovery Time	--	55	--	nS	IF=20A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	77	--	nC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 0.5%

Typical Feature Curve

Figure 1: Output Characteristics

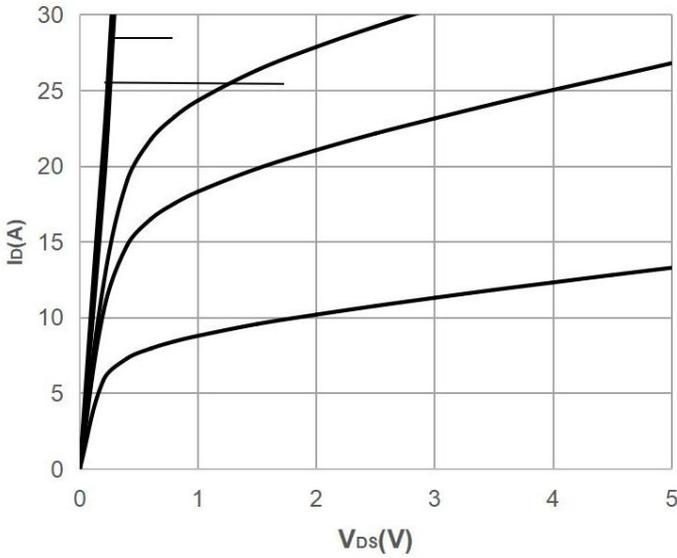


Figure 2: Typical Transfer Characteristics

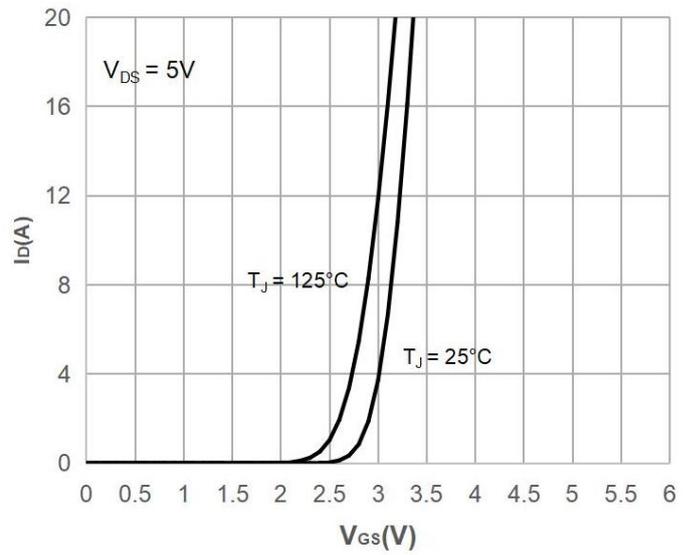


Figure 3: On-resistance vs. Drain Current

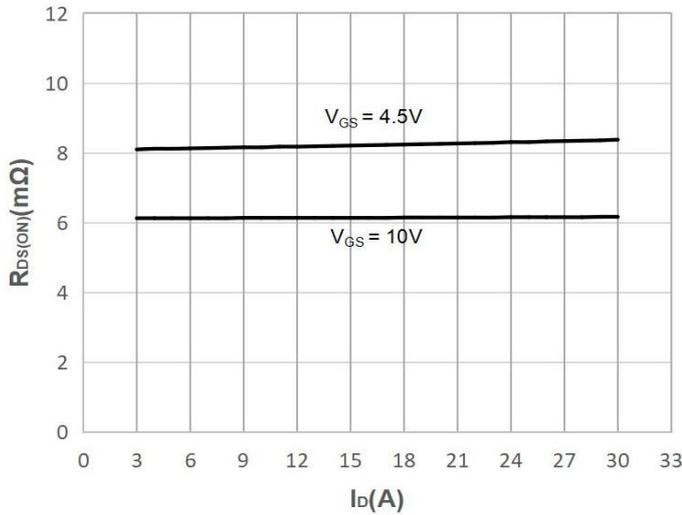


Figure 4: Body Diode Characteristics

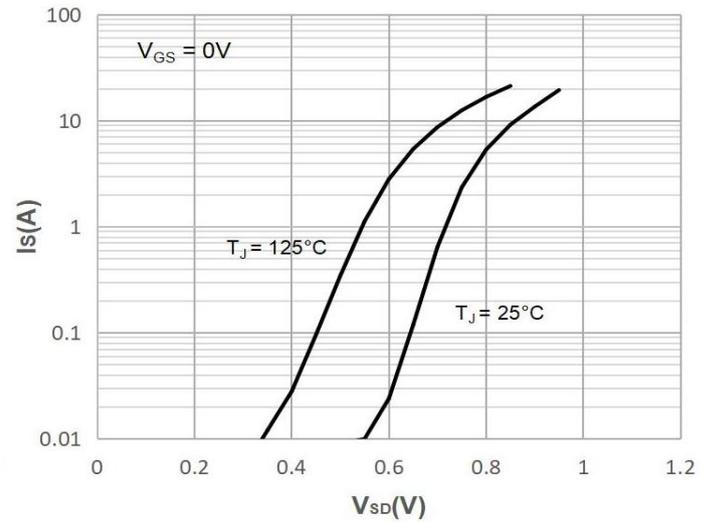


Figure 5: Gate Charge Characteristics

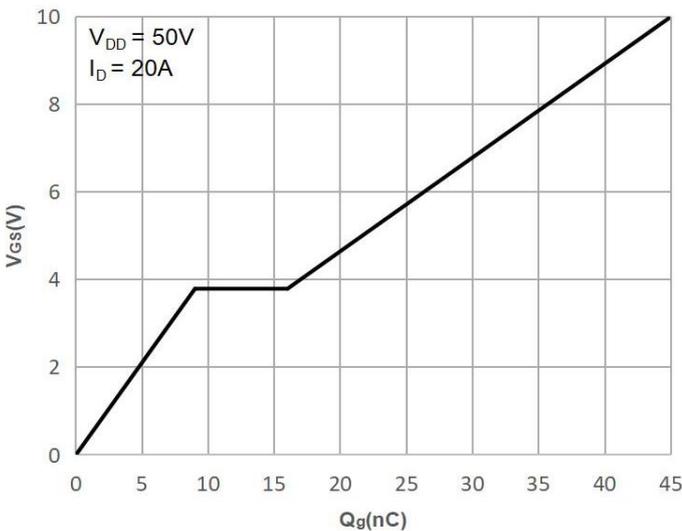


Figure 6: Capacitance Characteristics

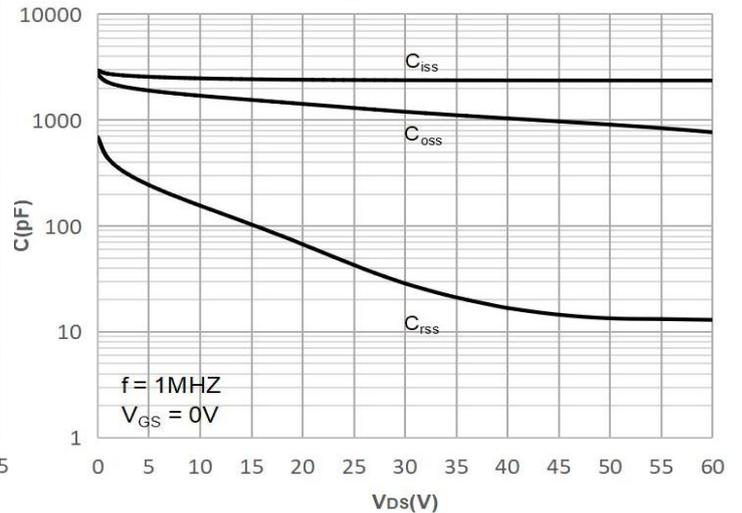


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

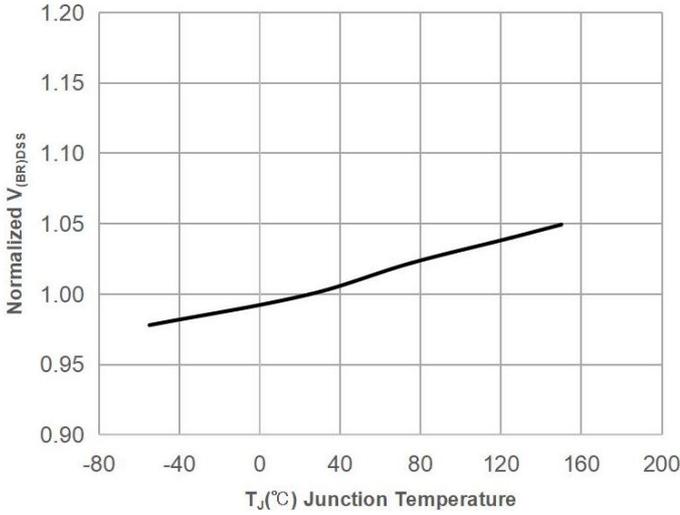


Figure 8: Normalized on Resistance vs. Junction Temperature

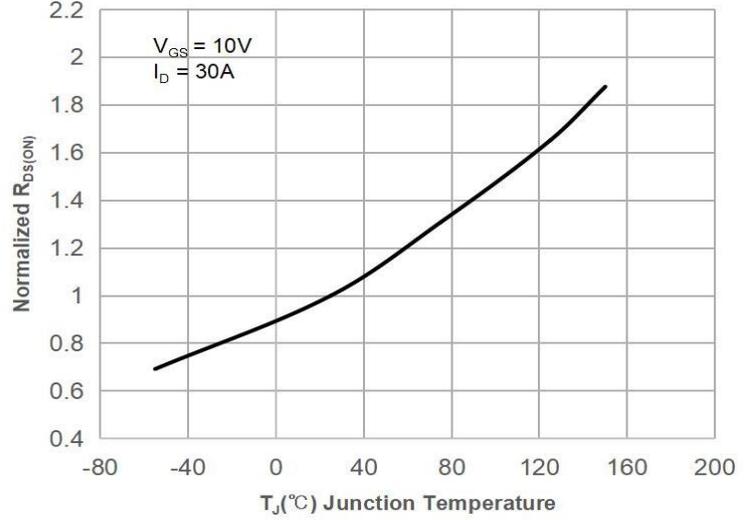


Figure 9: Maximum Safe Operating Area

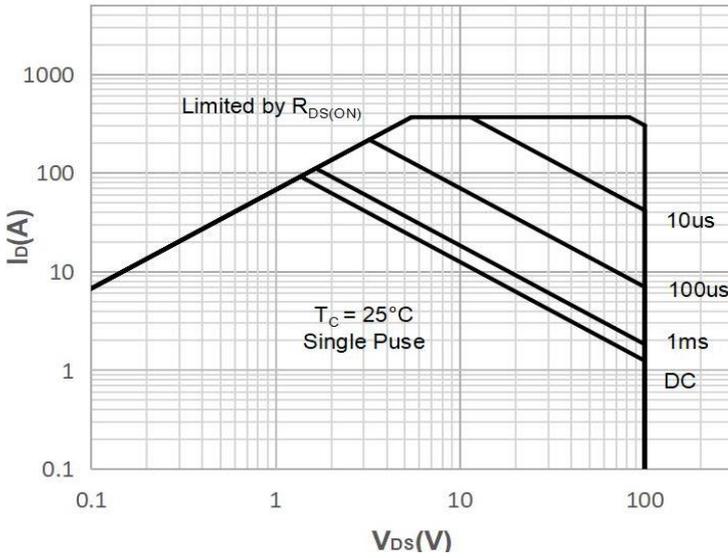


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

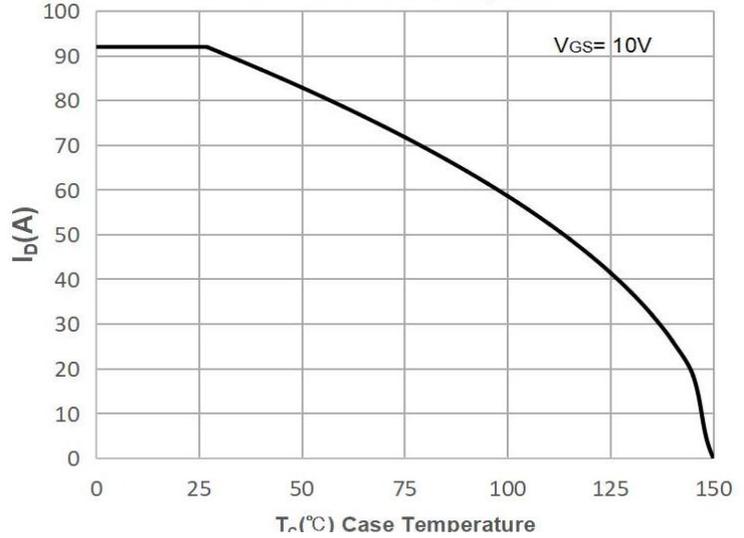


Figure 11: Normalized Maximum Transient Thermal Impedance

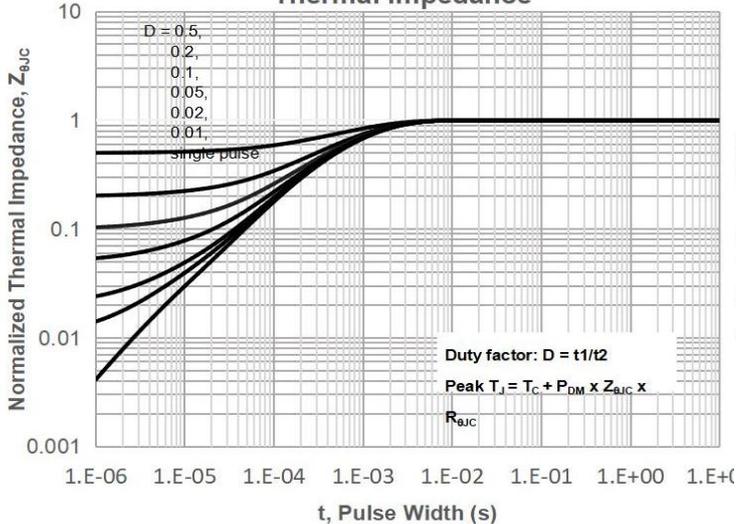
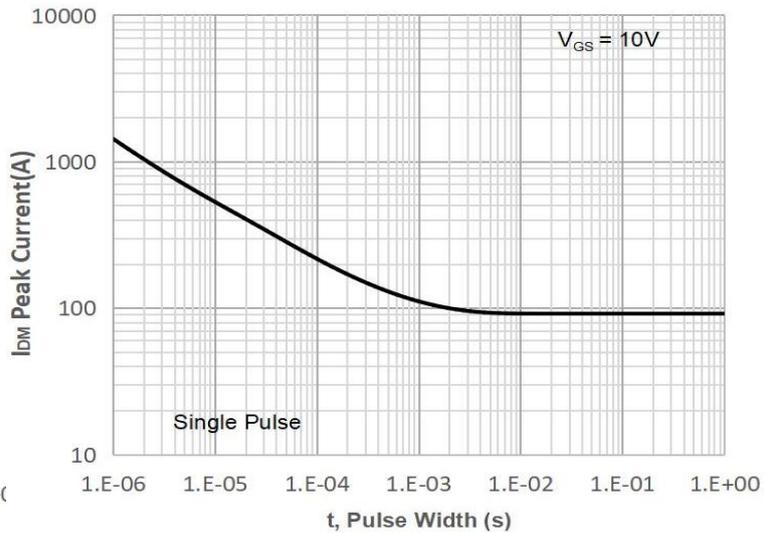
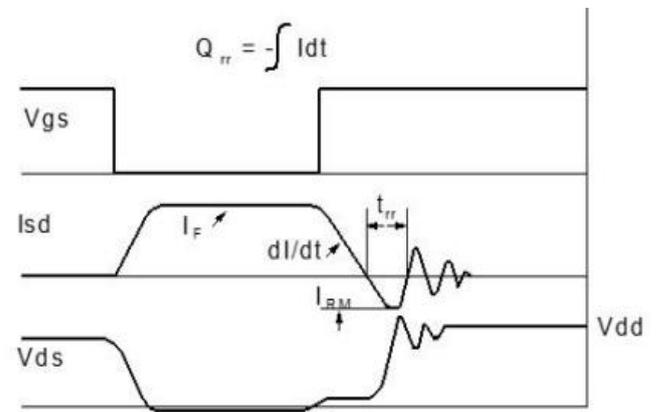
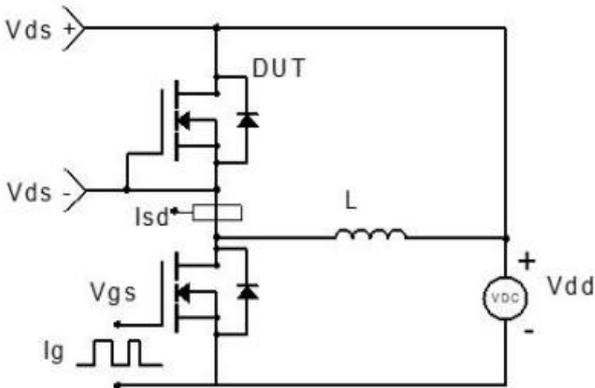
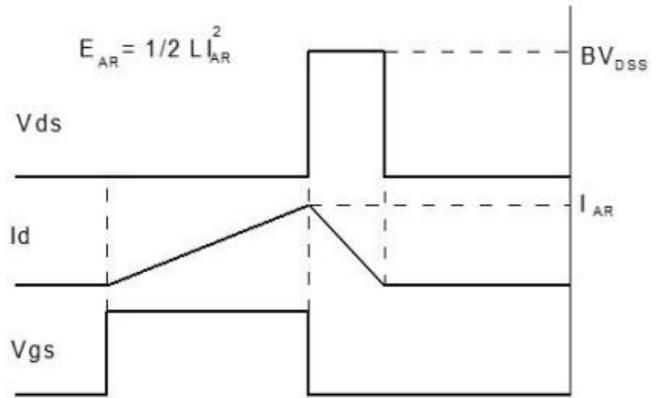
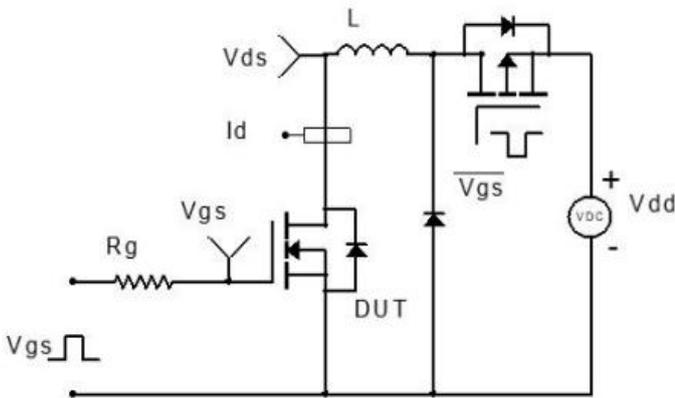
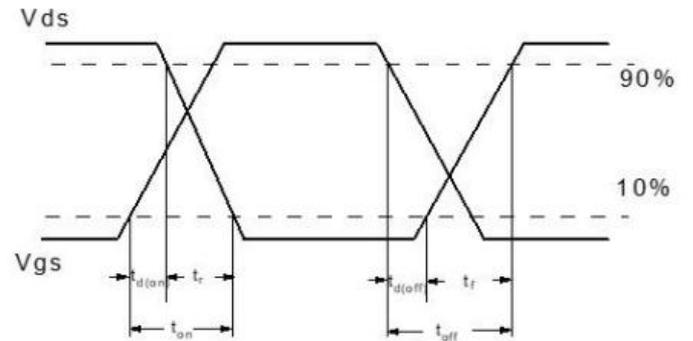
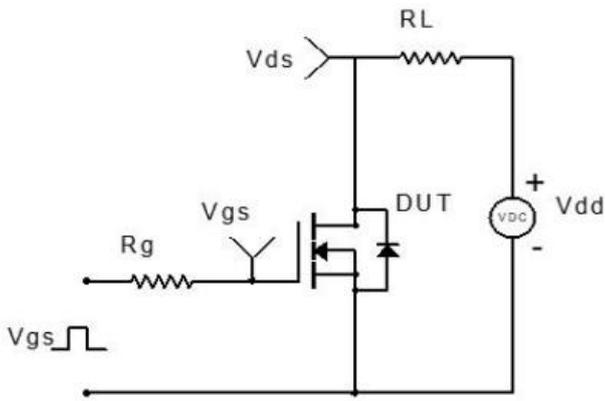
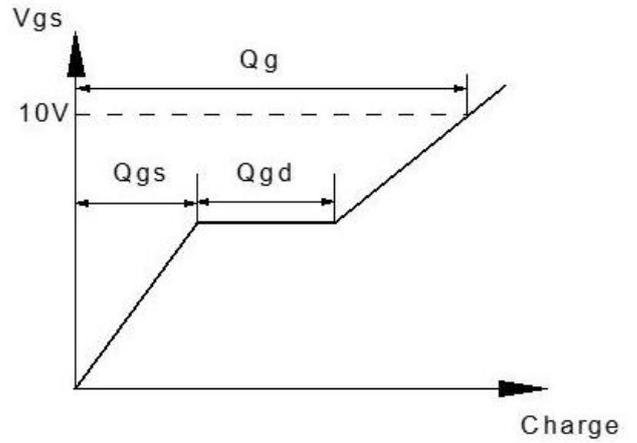
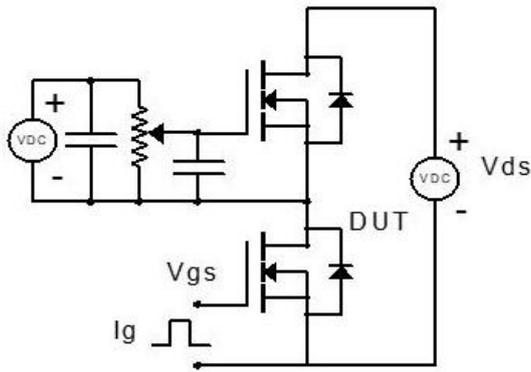
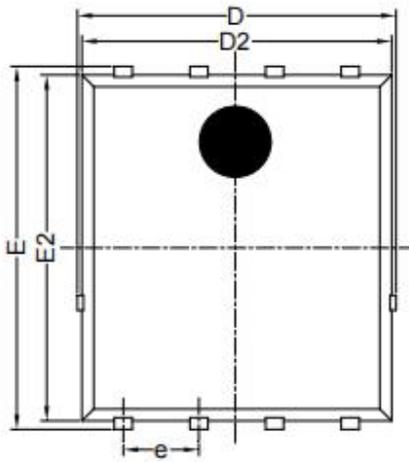
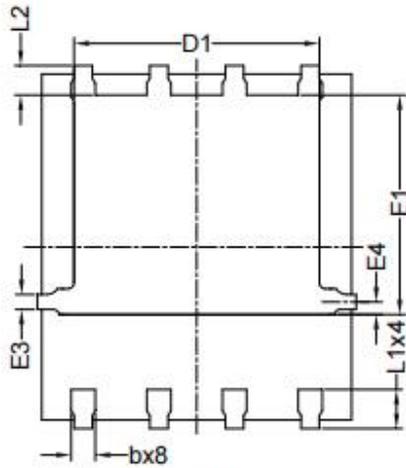
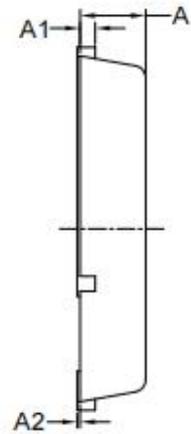
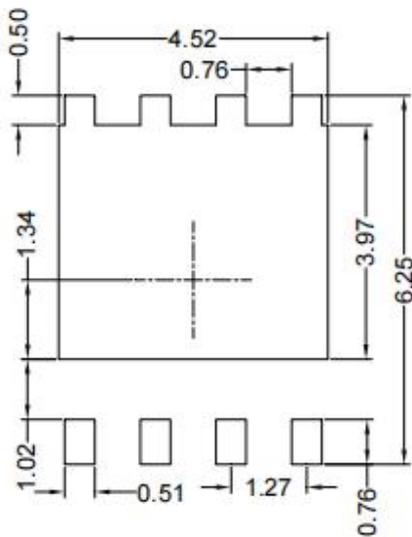


Figure 12: Peak Current Capacity



Test ircuits and Waveforms



Package outline drawing(DFN5*6 Unit: mm)

Top View
 正面视图

Bottom View
 背面视图

Side View
 侧面视图

Suggested Solder Pad Layout
 Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

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