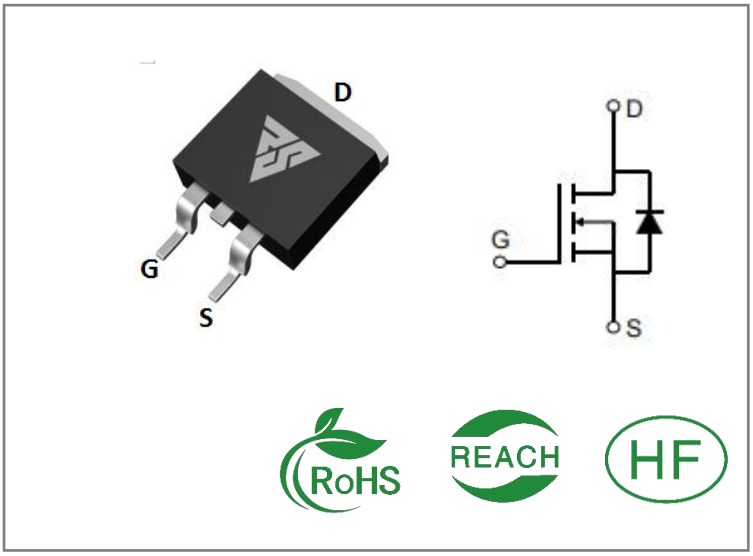
ID	R_{DS}(ON)(Typ)	VDSS
100A	7mΩ	120V



Applications:
- Load Switch
- PWM Applications
- Power Managment

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS120N100US	TO-263	120N100US	Tape&reel	800 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS120N100US	Units
VDSS	Drain-to-Source Voltage	120	V
ID	Continuous Drain Current TC=25℃	100	A
ID	Continuous Drain Current TC=100℃	54	
IDM	Pulsed Drain Current	360	
PD	Power Dissipation	140	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L=0.5mH,VDD=50V, VG=10V, RG=25Ω,IAS=30A,Tj = 25℃	225	mJ
TL TPKG	Maximum Temperature for Soldering	300	℃
	Leads at 0.063in(1.6mm)from Case for 10 S Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature
Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS120N100US	Units	Test Conditions
RθJC	Junction-to-Case	0.75	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	63		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	120	--	--	V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=120V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	7	8.5	mΩ	VGS=10V ID=30A
		--	7.7	9.9	mΩ	VGS=4.5V ID=20A
VGS (TH)	Gate Threshold Voltage	1.4	1.9	2.6	V	VGS=VDS ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	13	--	nS	VDD=60V ID=30A RG=6Ω VGS=10V
trise	Rise Time	--	25	--		
td(OFF)	Turn- OFF Delay Time	--	38	--		
tfall	Fall Time	--	34	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	3384	--	pF	VGS= 0V VDS=60V f=1MHz
Coss	Output Capacitance	--	644	--		
Crss	Reverse Transfer Capacitance	--	9.6	--		
Qg	Total Gate Charge	--	40	--	nC	VDS= 60V ID=20A VGS=10V
Qgs	Gate- to- Source Charge	--	9	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	10	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	100	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	400	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=30A VGS=0V
trr	Reverse Recovery Time	--	65	--	nS	IS=15A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	70	--	nC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 0.5%

Typical Feature Curve

Figure 1: Output Characteristics

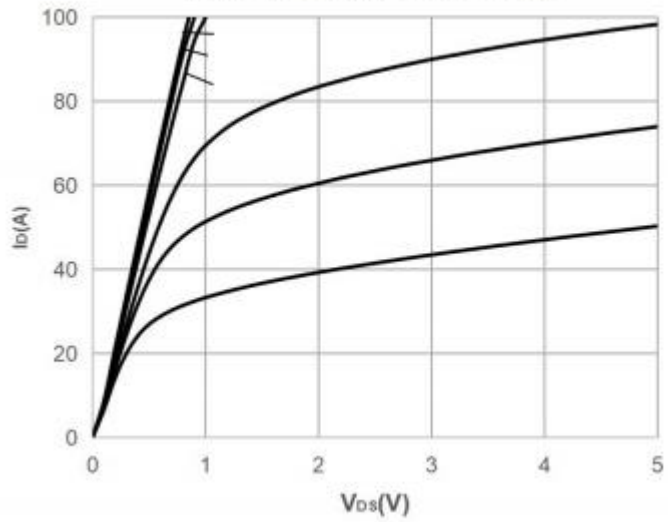


Figure 2: Typical Transfer Characteristics

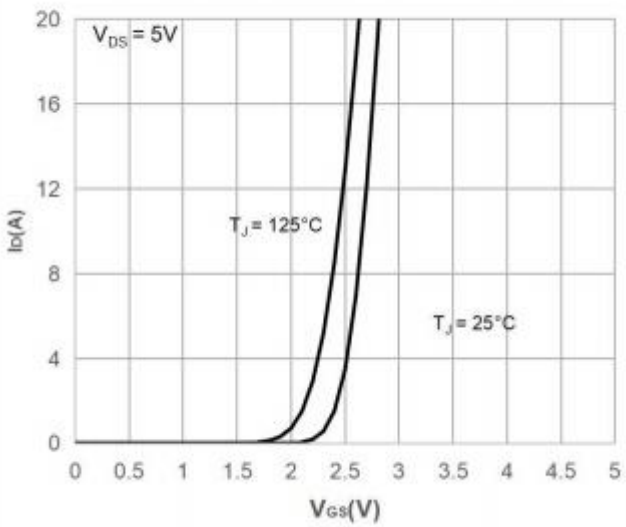


Figure 3: On-resistance vs. Drain Current

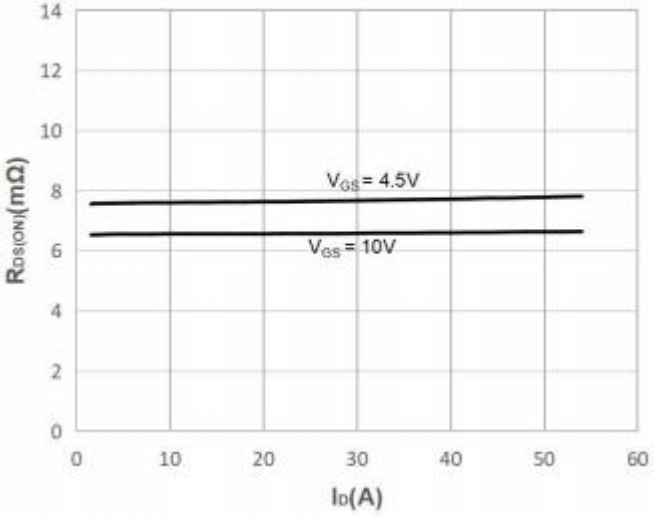


Figure 4: Body Diode Characteristics

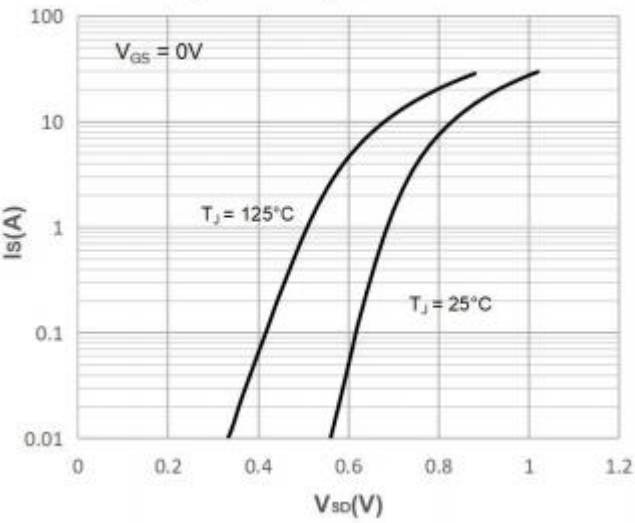


Figure 5: Gate Charge Characteristics

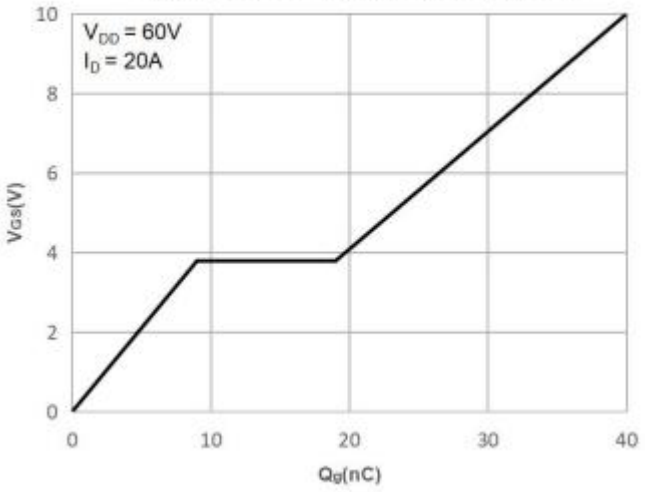


Figure 6: Capacitance Characteristics

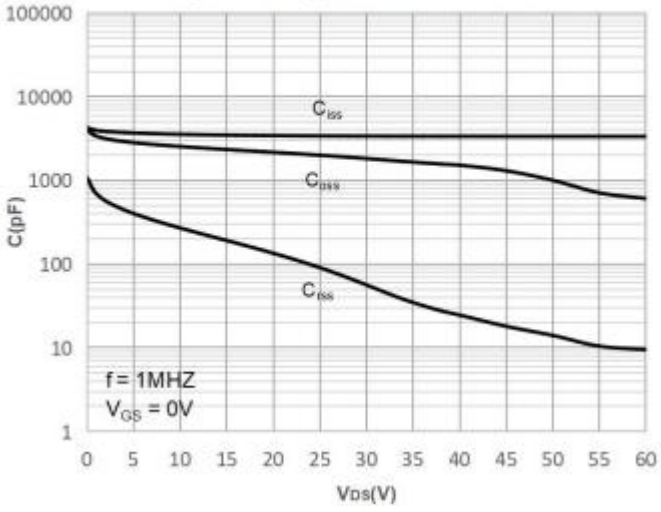


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

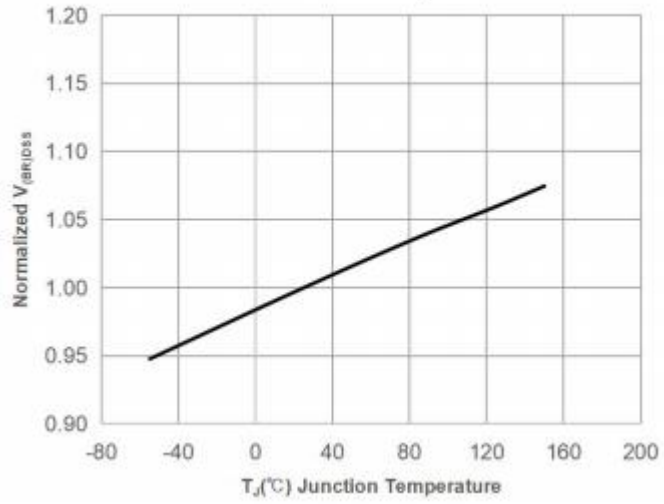


Figure 8: Normalized on Resistance vs. Junction Temperature

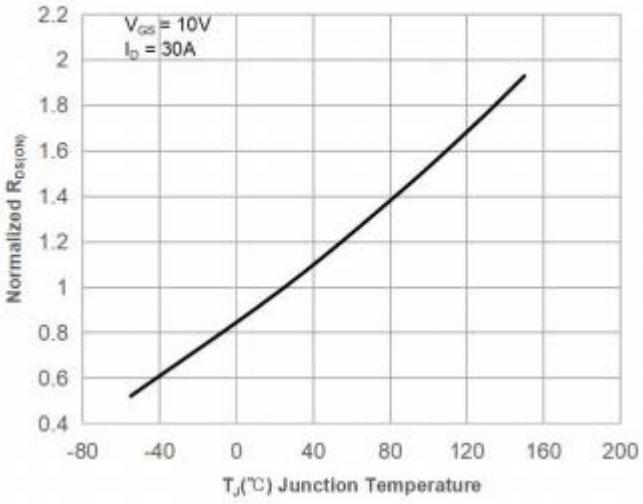


Figure 9: Maximum Safe Operating Area

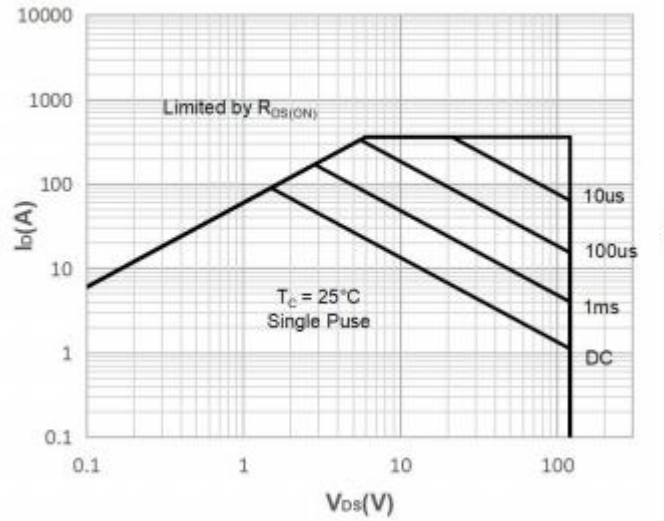


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

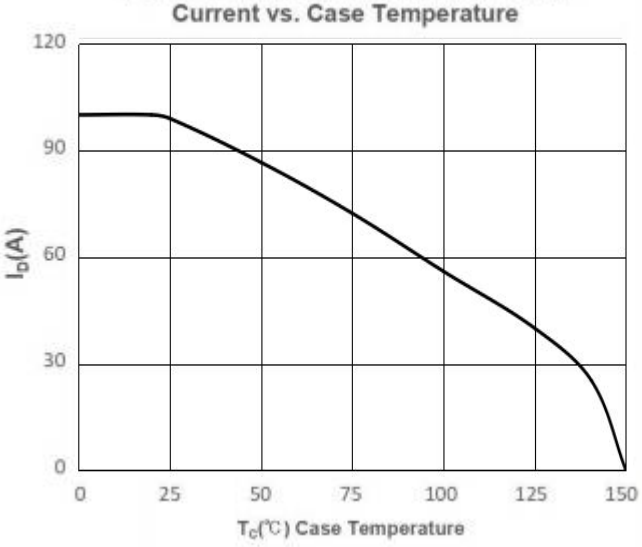


Figure 11: Normalized Maximum Transient Thermal Impedance

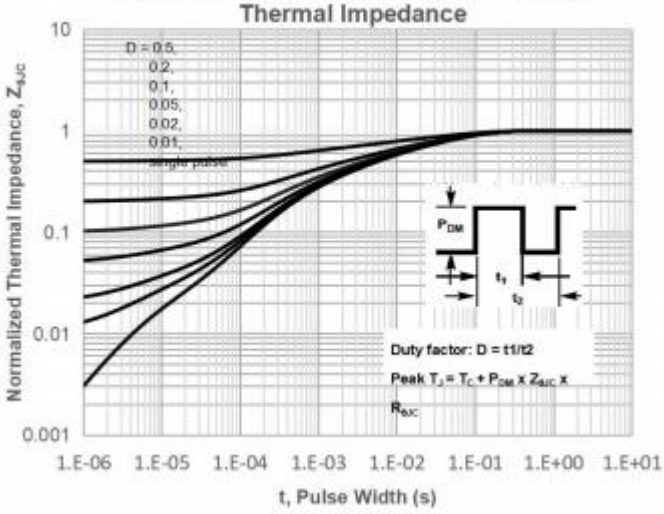
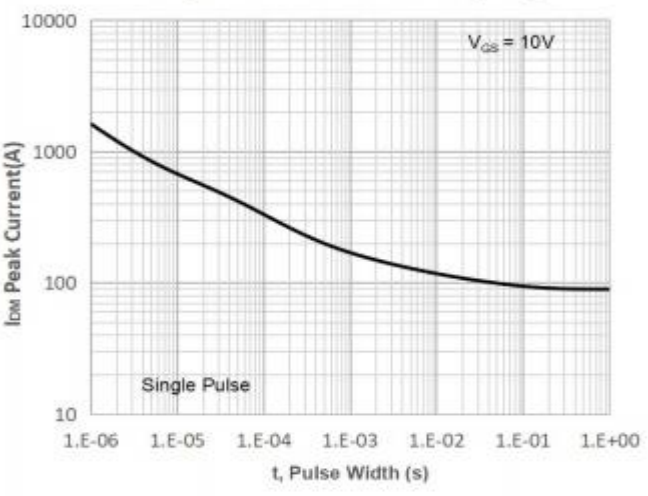
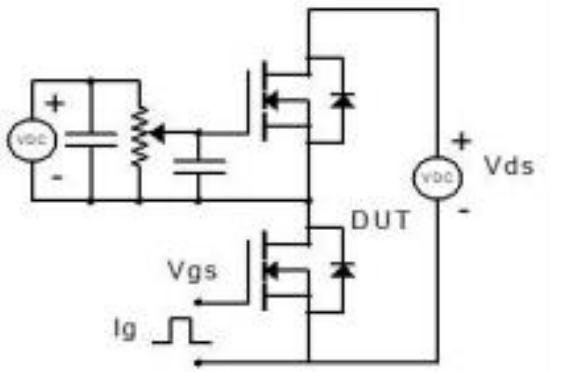
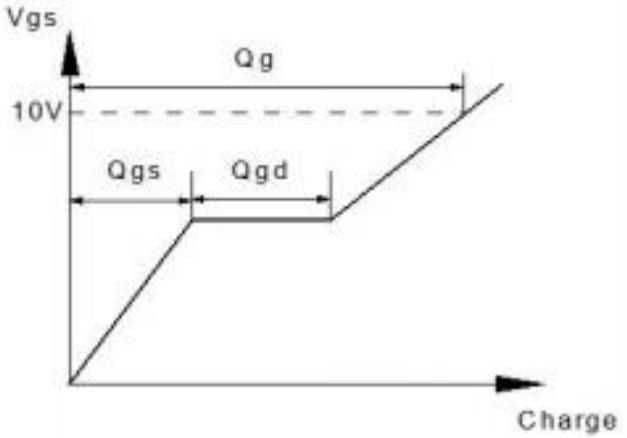


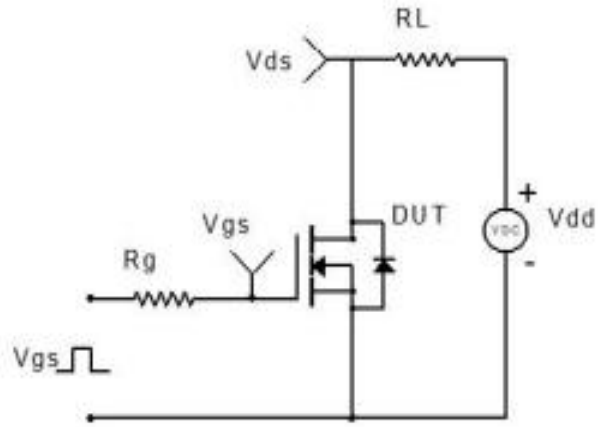
Figure 12: Peak Current Capacity

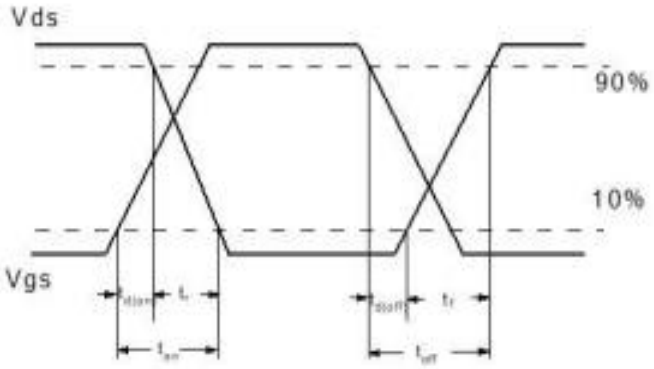


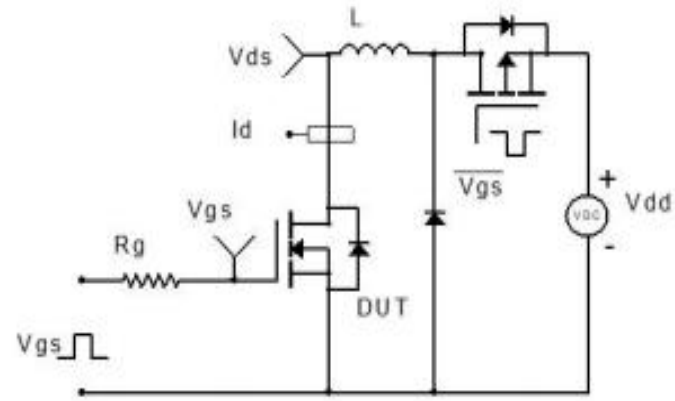
Test ircuits and Waveforms

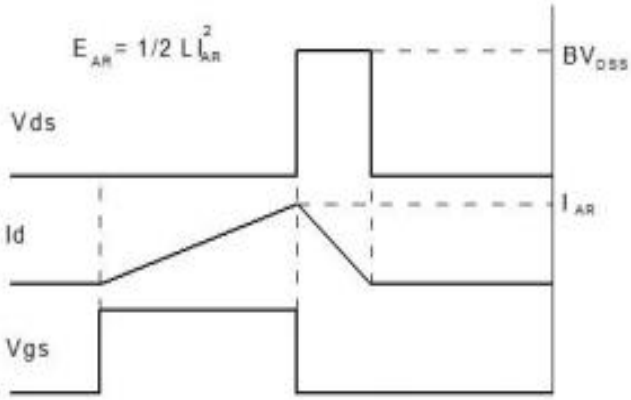


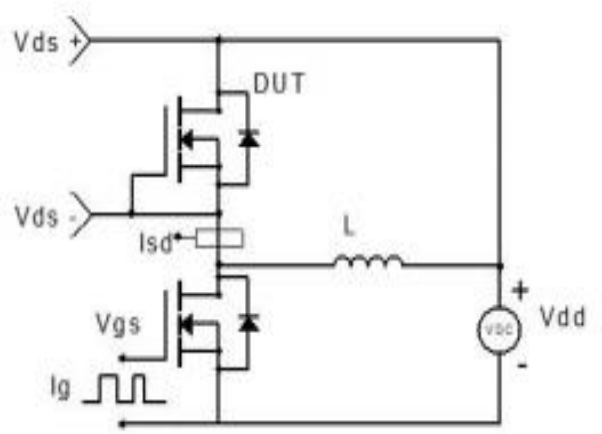


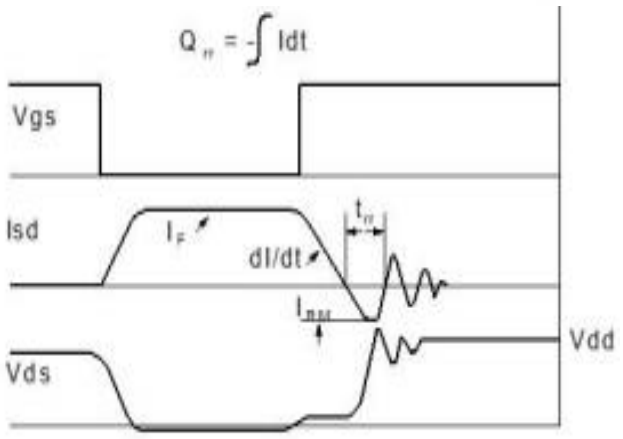




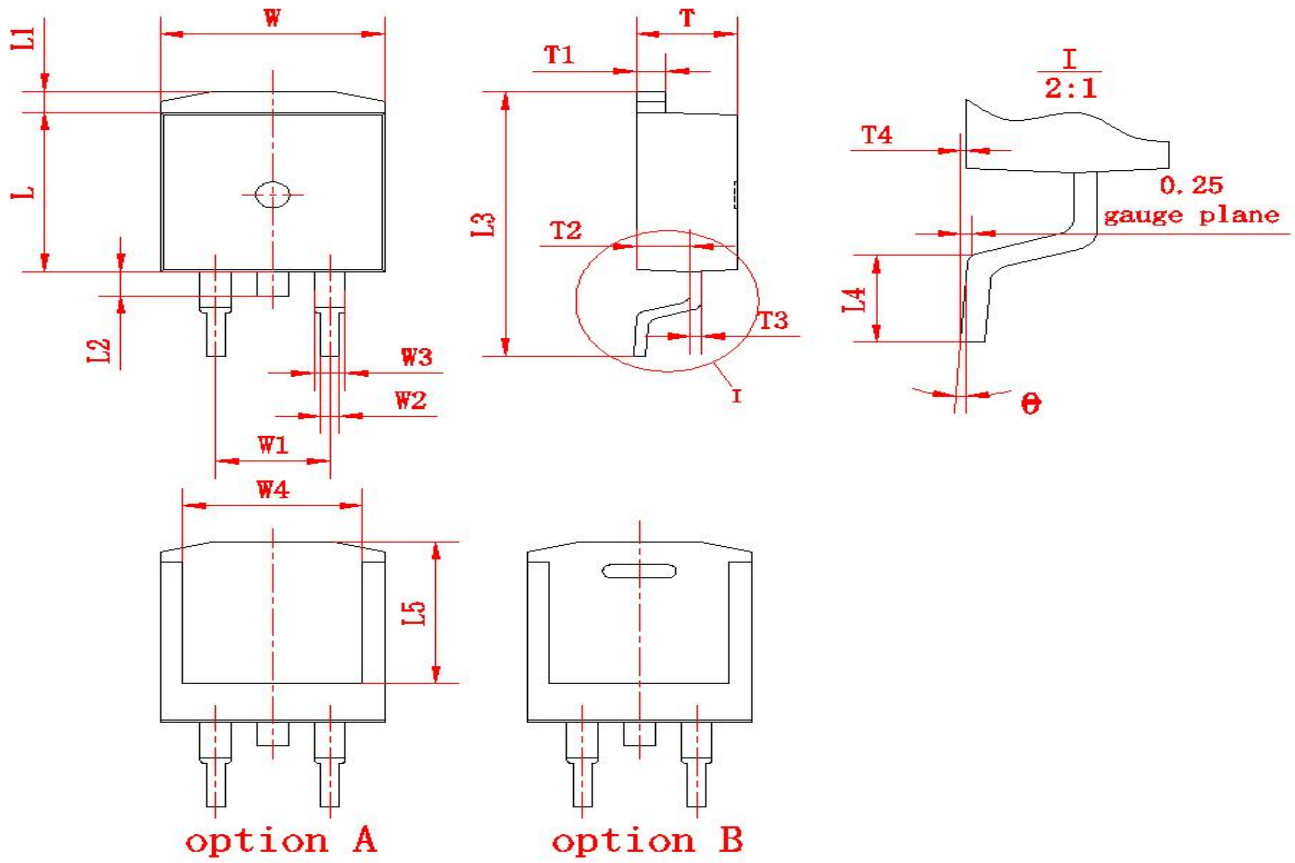








Package outline drawing(TO-263 Unit: mm)



（单位：mm）

符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	9.80	10.20	L1	1.00	1.40	T1	1.20	1.40
W1	(5.08)		L2	1.20	1.60	T2	2.20	2.60
W2	0.70	0.95	L3	15.00	15.60	T3	0.45	0.65
W3	1.17	1.62	L4	2.20	2.80	T4	0	0.25
W4	(8.0)		L5	(8.2)		θ	0°	8°
L	9.00	9.40	T	4.30	4.70			

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