

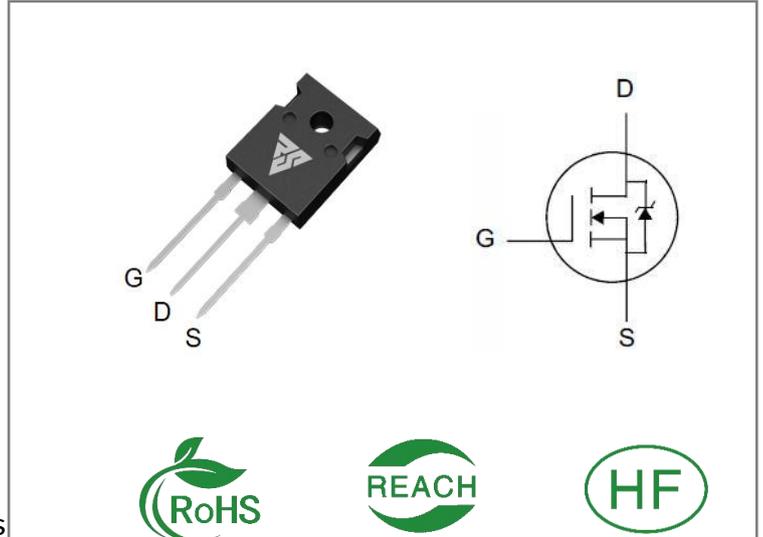
ID	R <sub>DS(ON)</sub> (Typ)	VDSS
200A	4.1mΩ	150V

**Applications:**

- Motor Drives
- BMS
- Synchronous Rectification

**Features:**

- Proprietary New Trench Technology
- R<sub>DS(ON)</sub>,typ.=4.1mΩ@V<sub>GS</sub>=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode


**Ordering Information**

Part Number	Package	Marking	Packing	Qty.
RS150N200UHW	T0-247-3	150N200UHW	Tube	30 PCS

**Absolute Maximum Ratings** T<sub>c</sub>= 25°C unless otherwise specified

Symbol	Parameter	RS150N200UHW	Units
VDSS	Drain-to-Source Voltage T <sub>J</sub> =+25°C to +150°C	150	V
ID	Continuous Drain Current T <sub>C</sub> =25°C	200	A
	Continuous Drain Current T <sub>C</sub> =100°C	154	A
IDM	Pulsed Drain Current (Note*1)	800	A
PD	Power Dissipation	463	W
		3.7	W/°C
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy L=0.5mH	1200	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds		
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

**Thermal Resistance**

Symbol	Parameter	RS150N200UHW	Units	Test Conditions
R $\theta$ JC	Junction-to-Case	0.26	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 150 $^{\circ}\text{C}$
R $\theta$ JA	Junction-to-Ambient	50		1 cubic foot chamber, free air.

**OFF Characteristics** T<sub>J</sub>= 25 $^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	150	--	--	V	VGS=0V ID=250 $\mu\text{A}$
IDSS	Drain- to- Source Leakage Current	--	--	1	$\mu\text{A}$	VDS=150V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

**ON Characteristics** T<sub>J</sub>=25 $^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	4.1	4.8	m $\Omega$	VGS=10V ID=30A
VGS (TH)	Gate Threshold Voltage	2.5	--	4.5	V	VGS=VDS ID=250 $\mu\text{A}$

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	58	--	nS	VDS=75V ID=30A VGS=10V RG=4.7 $\Omega$
trise	Rise Time	--	71	--		
td(OFF)	Turn- OFF Delay Time	--	88	--		
tfall	Fall Time	--	38	--		

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	10620	--	pF	VGS=0V VDS=100V f=1.0MHz
Coss	Output Capacitance	--	32	--		
Crss	Reverse Transfer Capacitance	--	867	--		
Qg	Total Gate Charge	--	154	--	nC	VDD=120V ID=30A VGS=10V
Qgs	Gate- to- Source Charge	--	60	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	36	--		
RG	Gate Series Resistance	--	2.0	--	Ω	f=1.0MHZ

**Source- Drain Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	200	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	800	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=50A,VGS=0V
trr	Reverse Recovery Time	--	114	--	nS	VGS=0V IF=30A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	403	--	nC	

**Notes:**

- \* 1. Repetitive rating, pulse width limited by maximum junction temperature.
- \* 2. Pulse Test: Pulse width ≤ 380μs, Duty Cycle ≤ 2%

Typical Feature Curve

Fig. 1. On-state characteristics

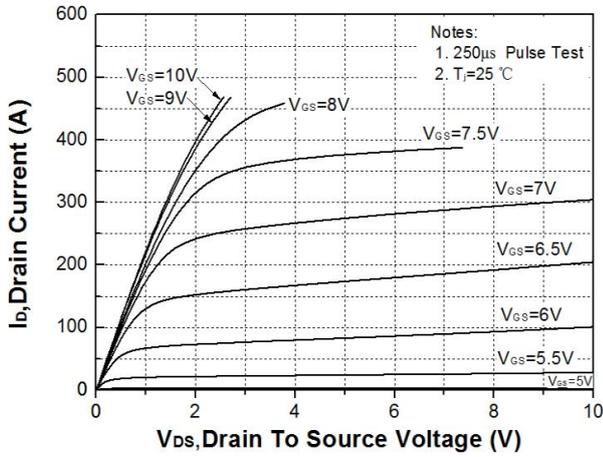


Fig. 2. Transfer Characteristics

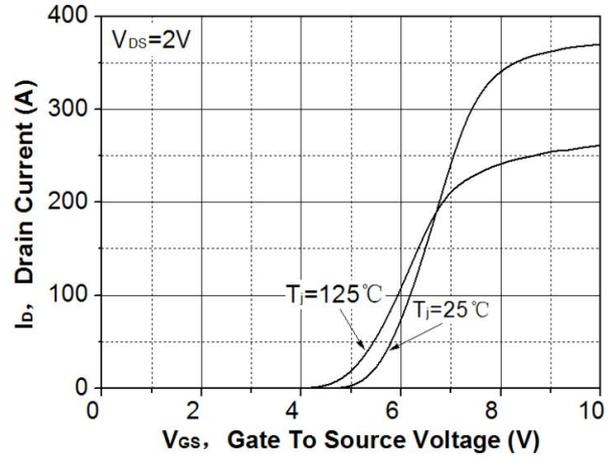


Fig. 3. On-resistance variation vs. drain current and gate voltage

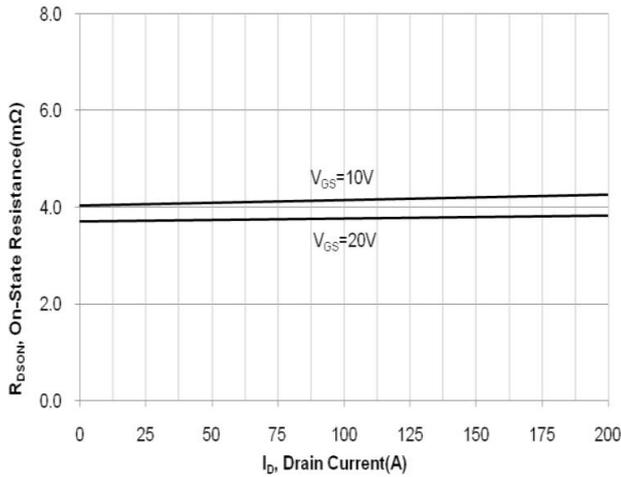


Fig. 4. On-state current vs. diode forward voltage

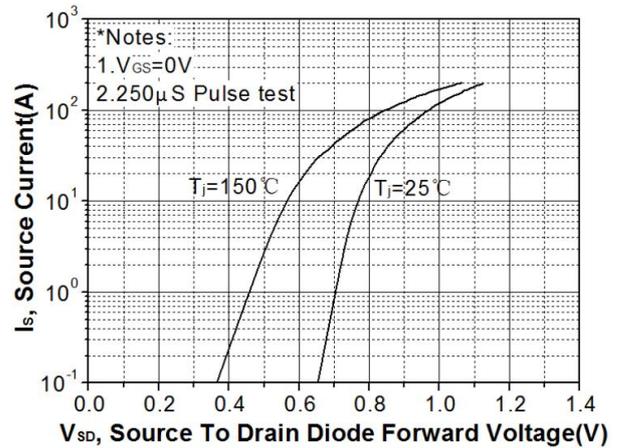


Fig 5. Breakdown voltage variation vs. junction temperature

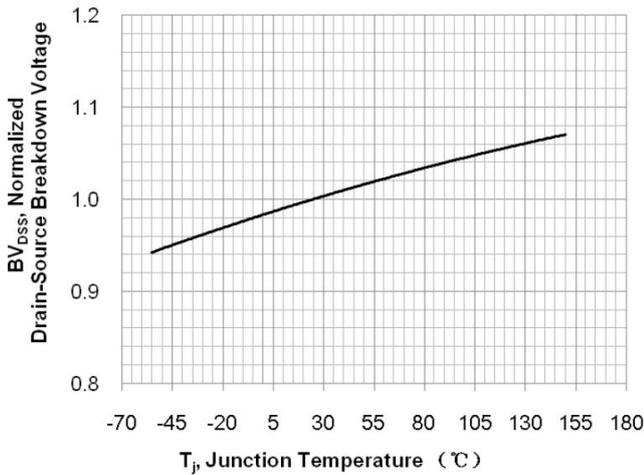
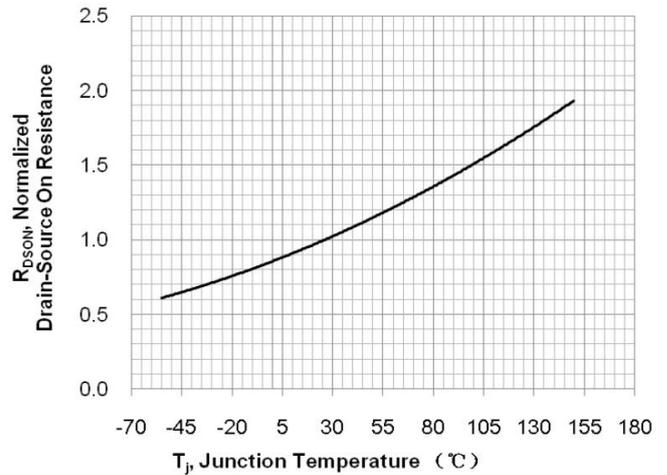
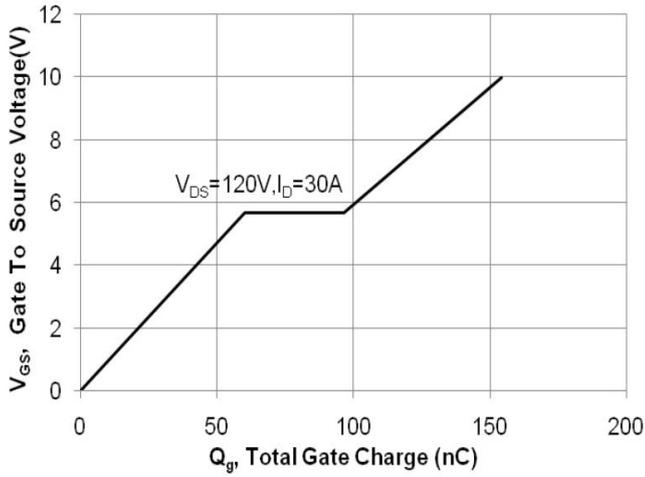


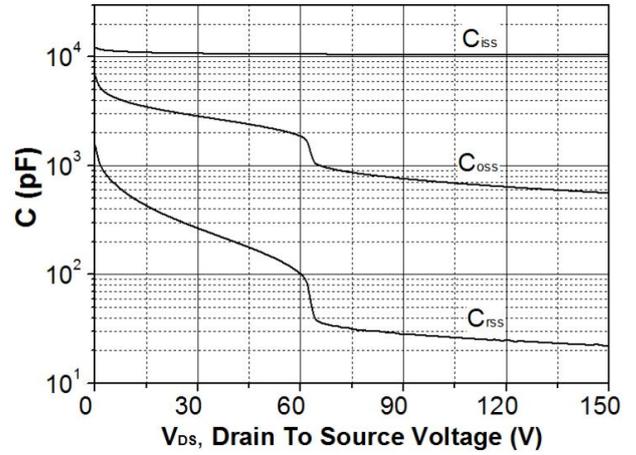
Fig. 6. On-resistance variation vs. junction temperature



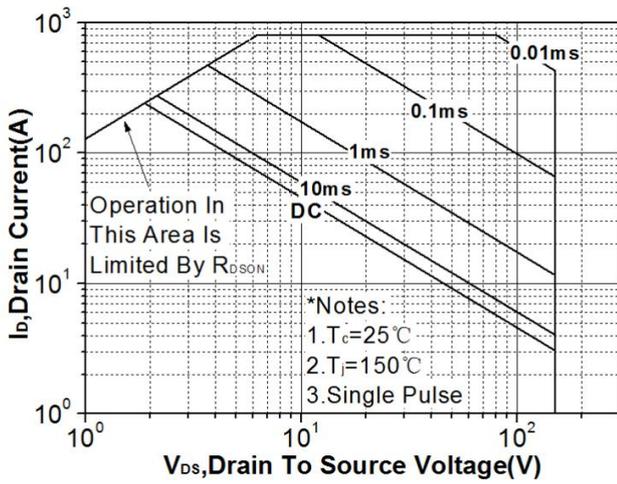
**Fig. 7. Gate charge characteristics**



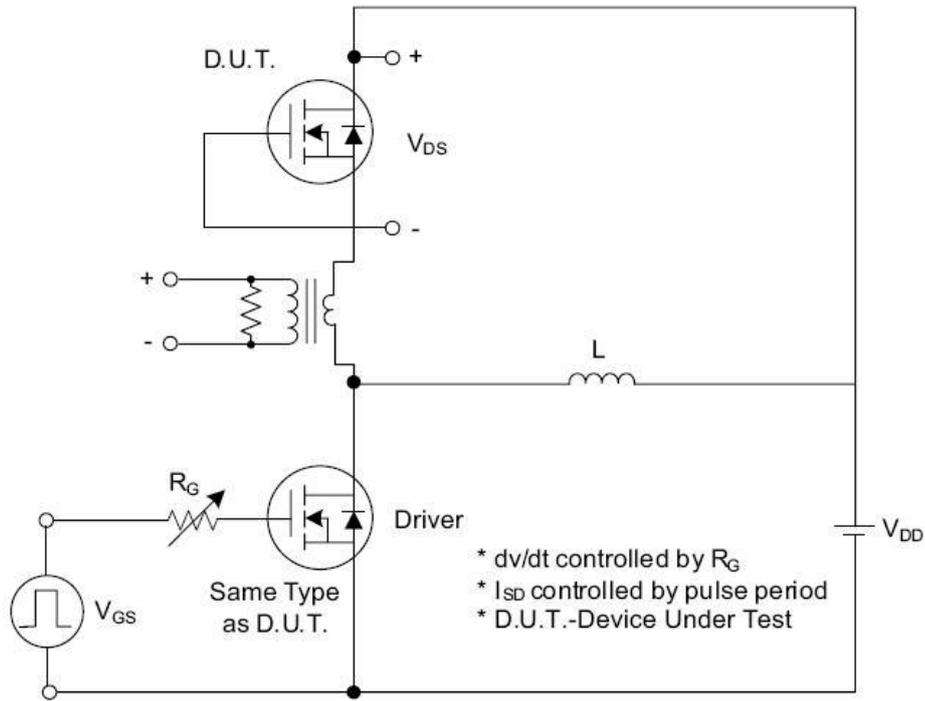
**Fig. 8. Capacitance Characteristics**



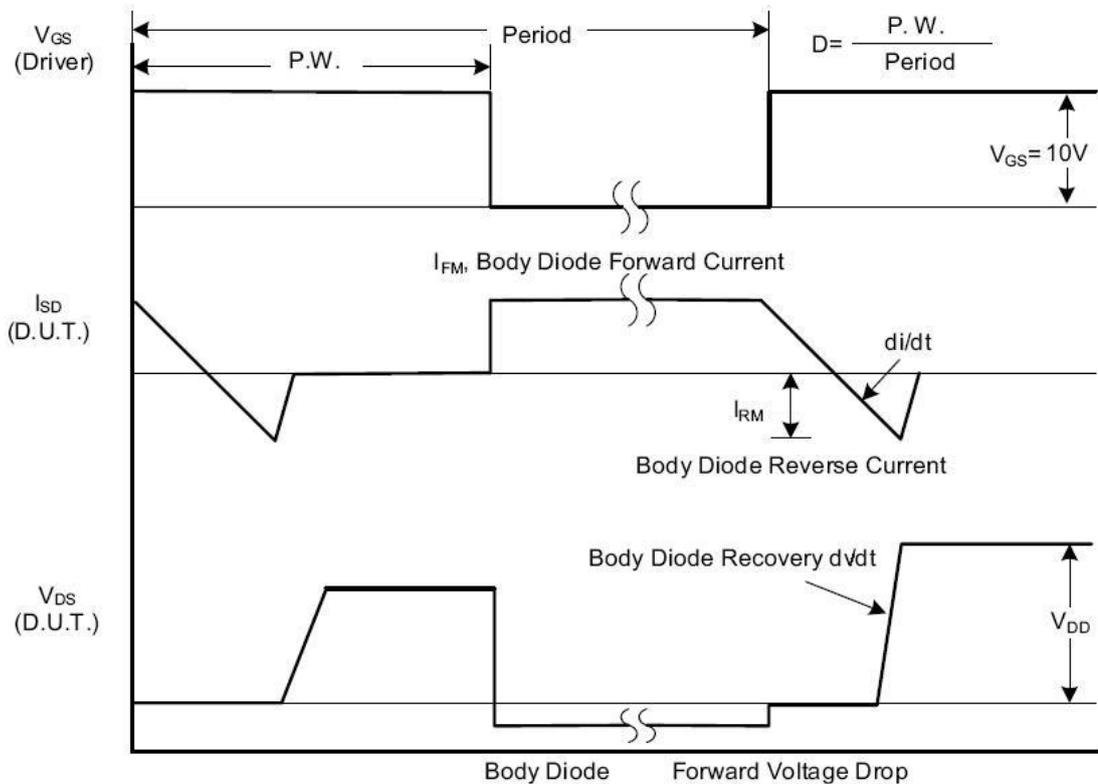
**Fig. 9. Maximum safe operating area**



**Test Circuits and Waveforms**



**Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit**



**Fig. 1.2 Peak Diode Recovery dv/dt Waveforms**

**Test Circuits and Waveforms**

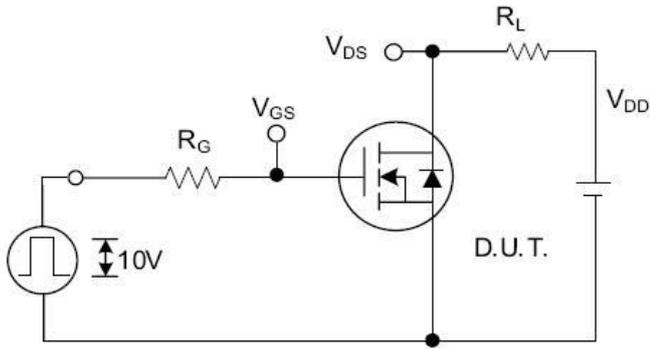


Fig. 2.1 Switching Test Circuit

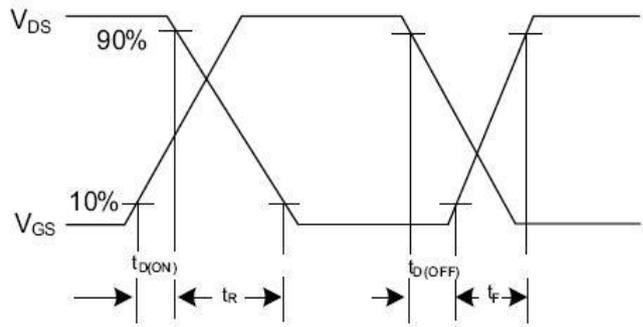


Fig. 2.2 Switching Waveforms

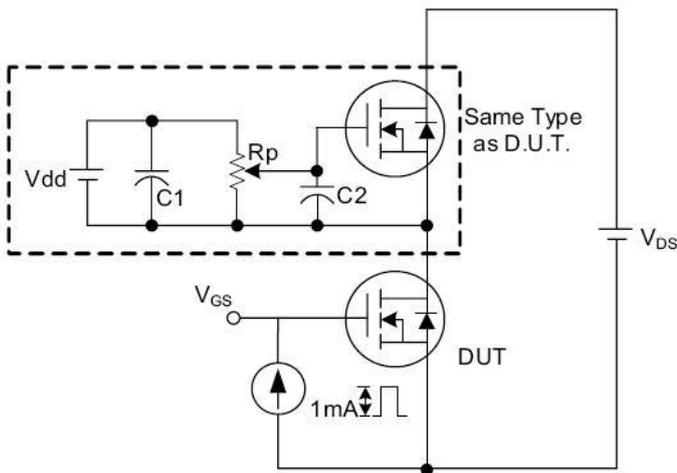


Fig. 3.1 Gate Charge Test Circuit

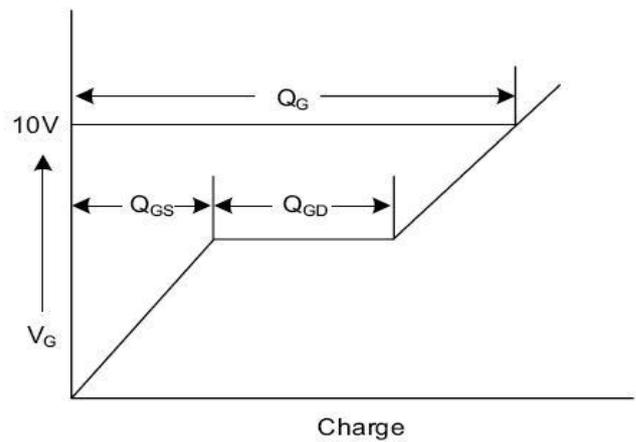


Fig. 3.2 Gate Charge Waveform

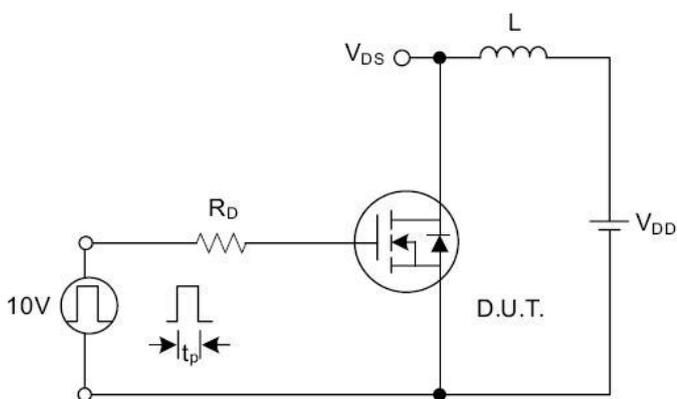


Fig. 4.1 Unclamped Inductive Switching Test Circuit

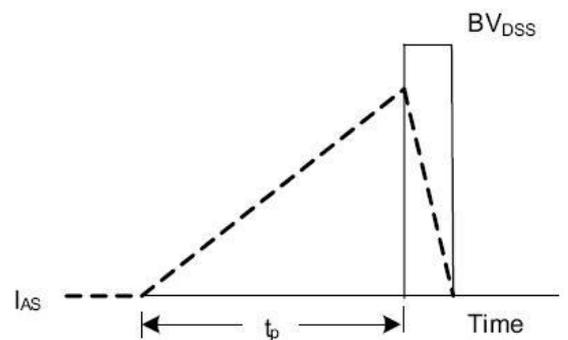
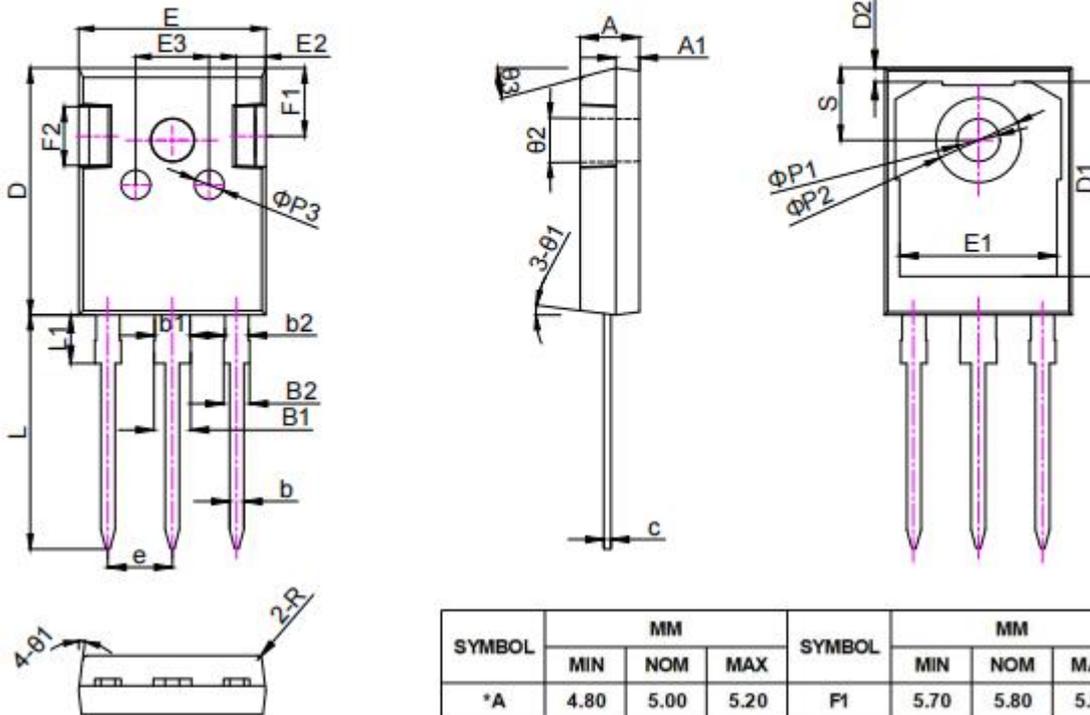


Fig. 4.2 Unclamped Inductive Switching Waveforms

**Package outline drawing(TO-247 Unit: mm )**


SYMBOL	MM			SYMBOL	MM		
	MIN	NOM	MAX		MIN	NOM	MAX
*A	4.80	5.00	5.20	F1	5.70	5.80	5.90
A1	1.90	2.00	2.10	F2	4.85	5.00	5.15
*b	1.10	1.20	1.30	*e	5.39	5.44	5.49
b1	2.90	3.00	3.10	*L	19.72	19.92	20.12
b2	1.95	2.00	2.05	*L1	4.03	4.13	4.23
*B1	3.00	3.10	3.20	$\theta 1$	5°	7°	9°
*B2	2.00	2.10	2.20	$\theta 2$	1°	2°	3°
*c	0.50	0.6	0.70	$\theta 3$	13°	15°	17°
*D	20.80	21	21.20	* $\Phi P1$	3.50	3.60	3.70
D1	16.40	16.55	16.70	$\Phi P2$	7.09	7.19	7.29
D2	1.07	1.17	1.27	$\Phi P3$	2.40	2.50	2.60
*E	15.60	15.80	16.00	*Q1	2.31	2.41	2.51
E1	13.11	13.26	13.41	S	6.05	6.15	6.25
E2	2.40	2.50	2.60	R	0.30	0.40	0.50
E3	6.10	6.20	6.30	带*为关键检验尺寸			

注:  
 1.表面粗糙度  $Ra = 1.14 \pm 0.20 \mu m$   
 2.带\*为关键检验尺寸

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