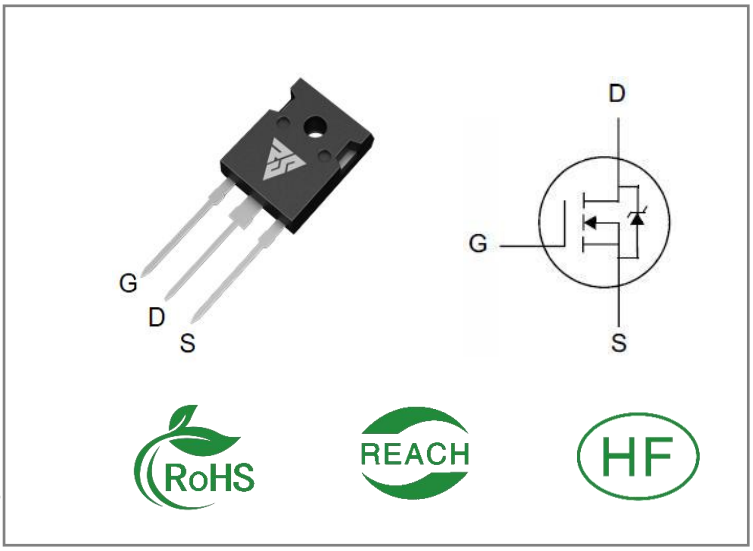
ID	R_{DS}(ON)(Typ)	VDSS
110A	9.3mΩ	200V



Applications:

- C/DC Converter
- Ideal for high-frequency switching and synchronous rectification

Features:

- Proprietary New Trench Technology
- RDS(ON),typ.=9.3mΩ@VGS=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS110N20UHW	T0-247-3	110N20UHW	Tube	30 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS110N20UHW	Units
VDSS	Drain-to-Source Voltage TJ=+25℃ to +150℃	200	V
ID	Continuous Drain Current TC=25℃	110	A
	Continuous Drain Current TC=100℃	75	A
IDM	Pulsed Drain Current (Note*1)	440	
PD	Power Dissipation	278	W
		2.22	W/℃
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L=10mH	2000	mJ
Dv/dt	Peak Diode Recovery dv/dt ISD= 9A di/dt < 100 A/μs, VDD < BVDSS,TJ=+150℃.	5	V/ns
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS110N20UHW	Units	Test Conditions
RθJC	Junction-to-Case	0.45	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	50		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	200	--	--	V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=200V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	9.3	10.5	mΩ	VGS=10V ID=35A
VGS (TH)	Gate Threshold Voltage	2.5	--	4.5	V	VGS=VDS ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	46	--	nS	VDS=100V ID=55A VGS=10V RG=4.7Ω
trise	Rise Time	--	21	--		
td(OFF)	Turn- OFF Delay Time	--	88	--		
tfall	Fall Time	--	18	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	10656	--	pF	VGS=0V VDS=100V f=1.0MHz
Coss	Output Capacitance	--	16	--		
Crss	Reverse Transfer Capacitance	--	389	--		
Qg	Total Gate Charge	--	145	--	nC	VDD=100V ID=55A VGS=10V
Qgs	Gate- to- Source Charge	--	49	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	27	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	110	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	440	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=70A,VGS=0V
trr	Reverse Recovery Time	--	185	--	nS	IF=55A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	469	--	nC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 380μs, Duty Cycle ≤ 2%

Typical Feature Curve

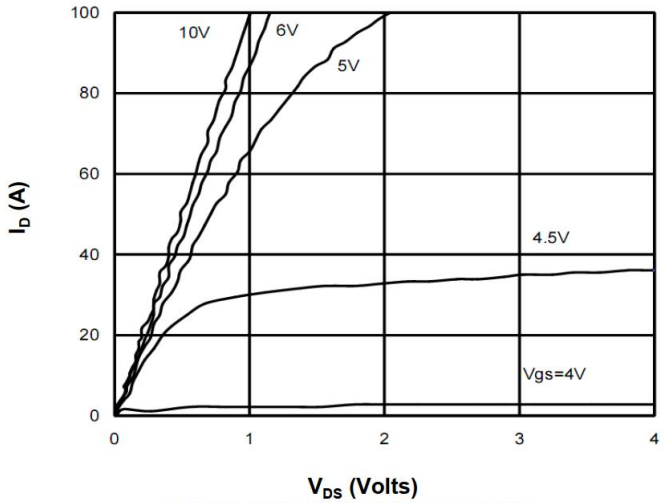


Figure 1: On-Region Characteristics

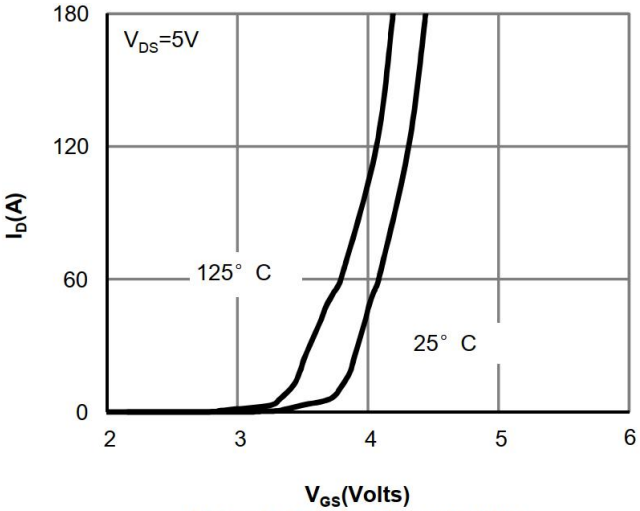


Figure 2: Transfer Characteristics

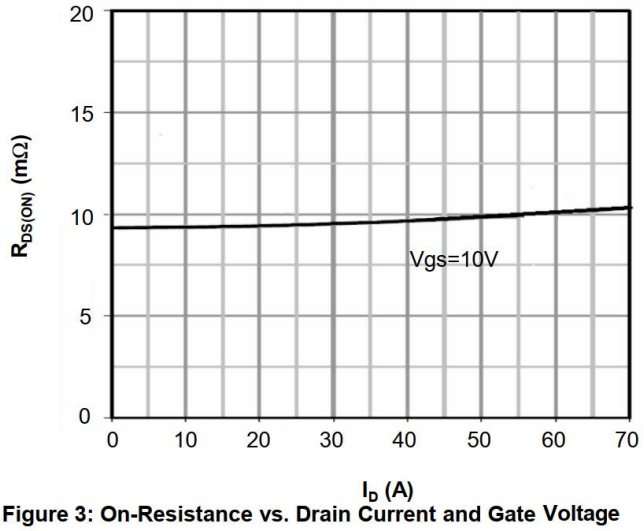


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

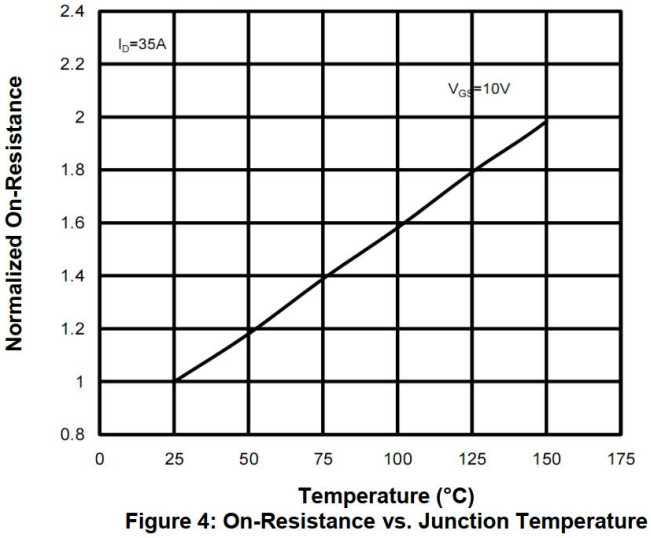


Figure 4: On-Resistance vs. Junction Temperature

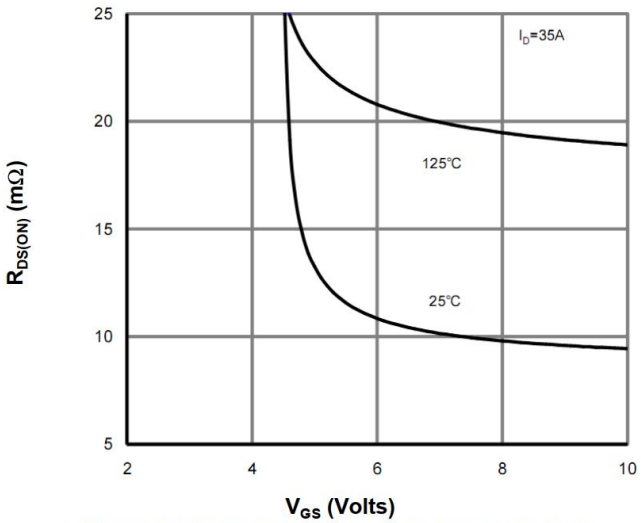


Figure 5: On-Resistance vs. Gate-Source Voltage

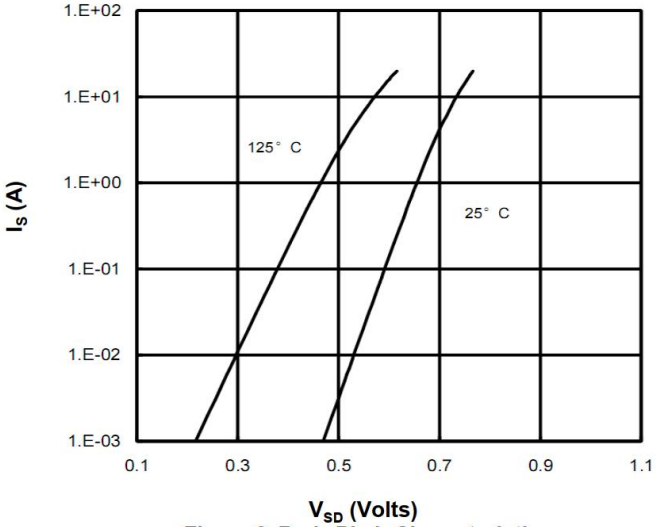


Figure 6: Body-Diode Characteristics

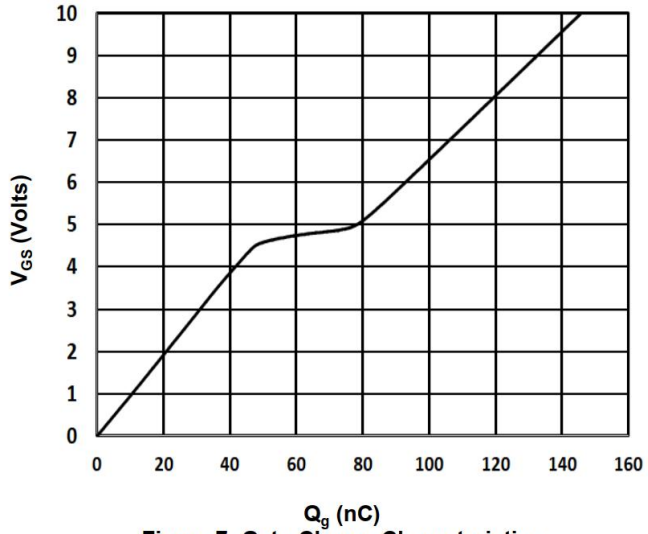


Figure 7: Gate-Charge Characteristics

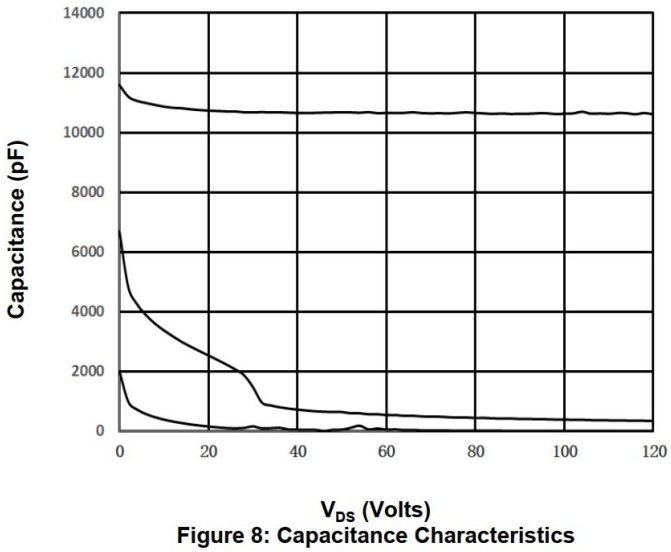


Figure 8: Capacitance Characteristics

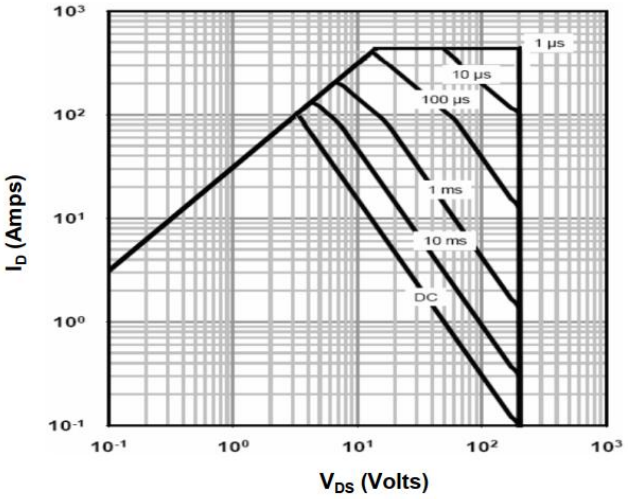


Figure 9: Maximum Forward Biased Safe Operating Area

Test Circuits and Waveforms

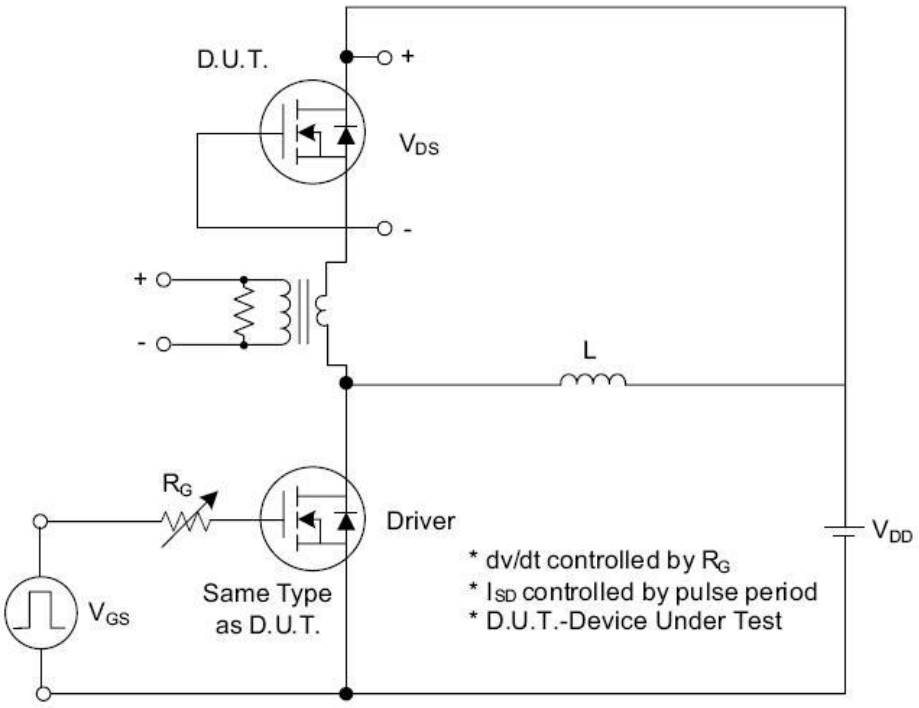


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

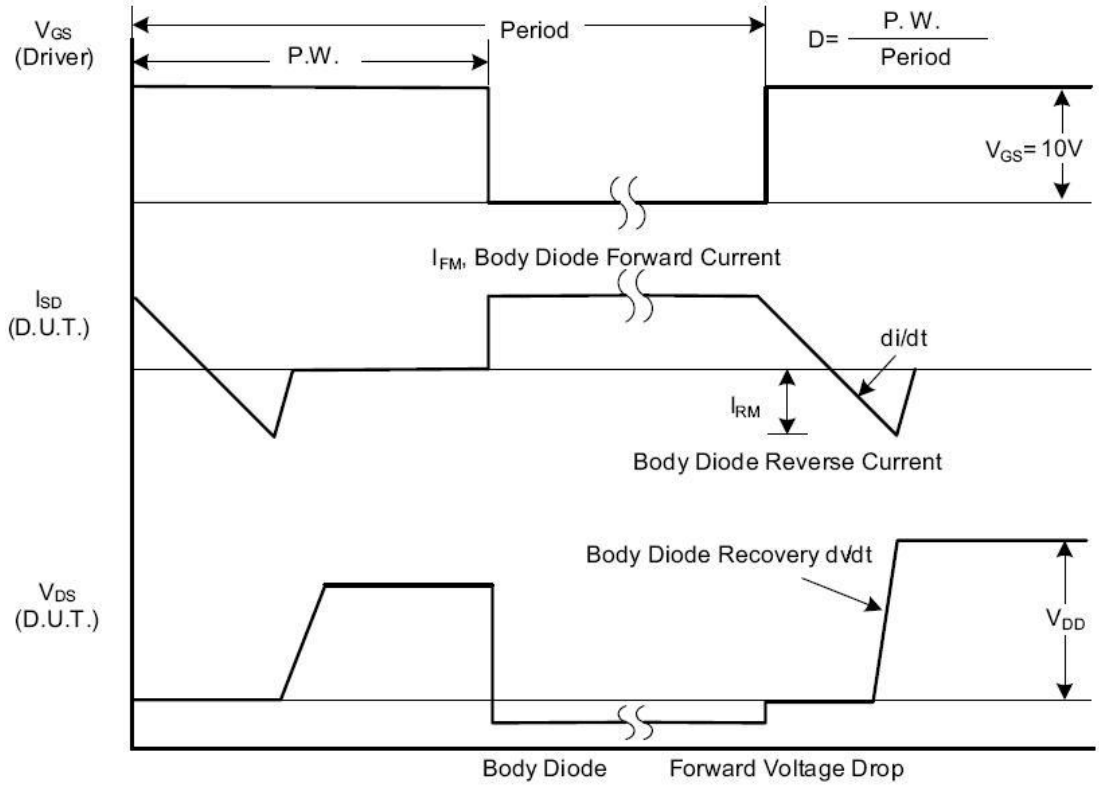


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms

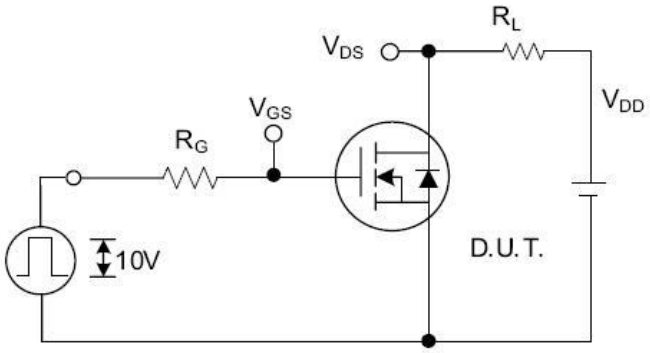


Fig. 2.1 Switching Test Circuit

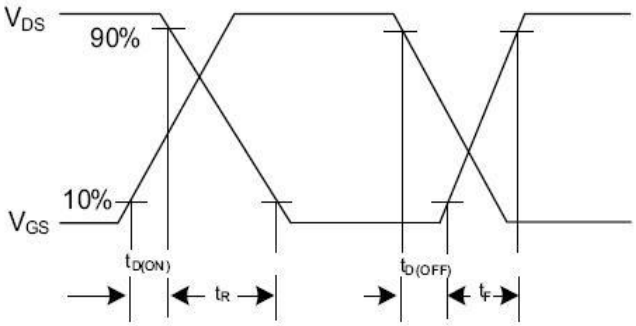


Fig. 2.2 Switching Waveforms

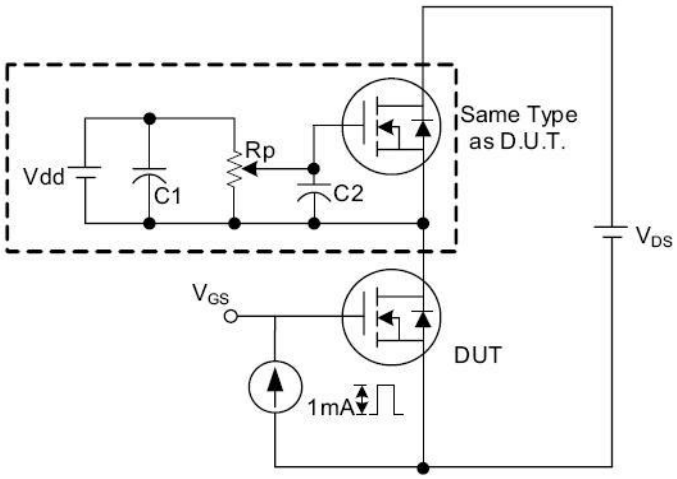


Fig. 3 . 1 Gate Charge Test Circuit

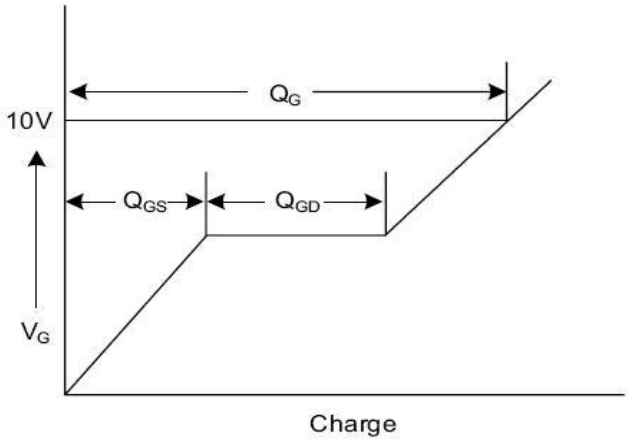


Fig. 3 . 2 Gate Charge Waveform

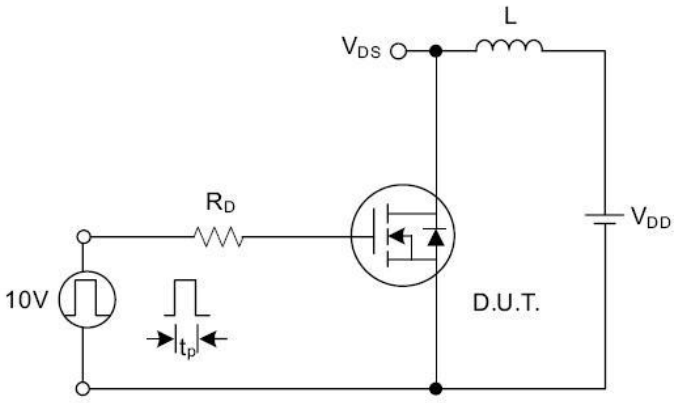


Fig. 4.1 Unclamped Inductive Switching Test Circuit

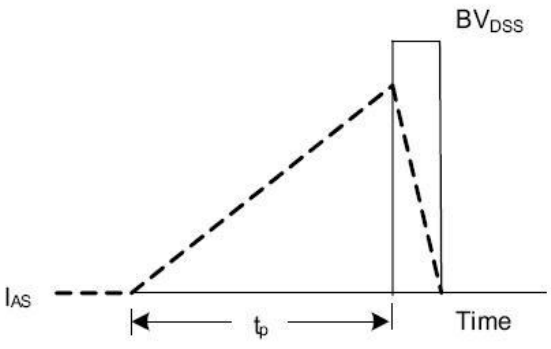
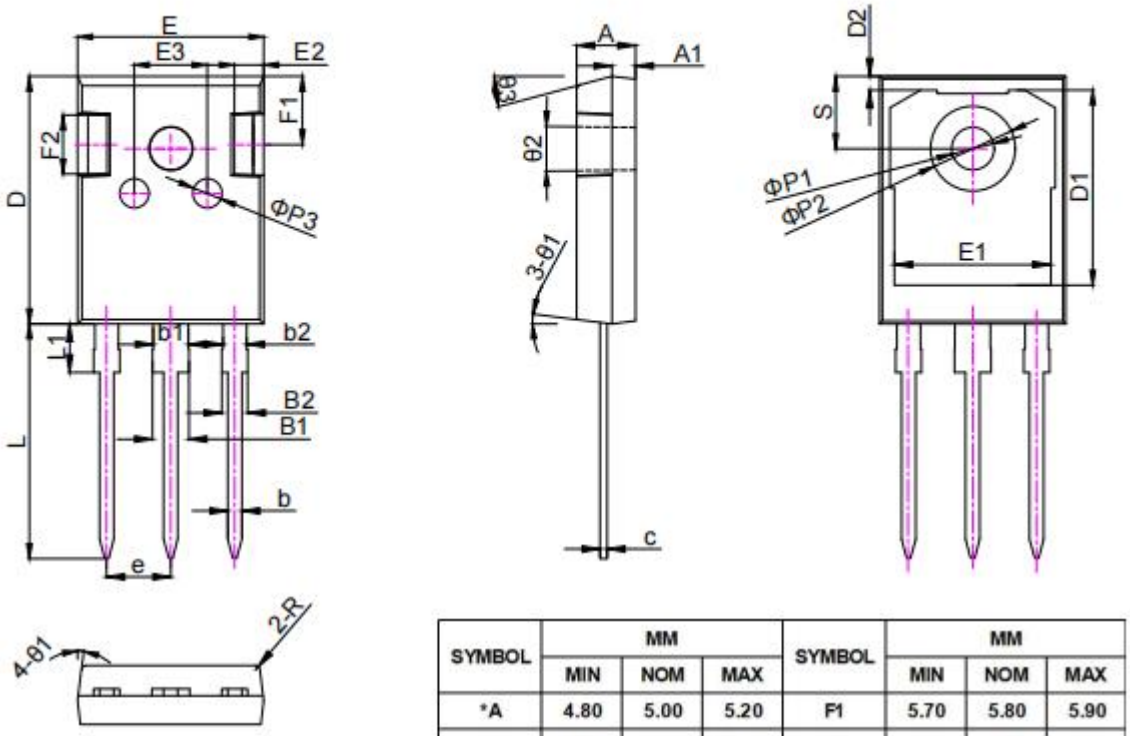


Fig. 4.2 Unclamped Inductive Switching Waveforms

Package outline drawing(TO-247 Unit: mm)



SYMBOL	MM			SYMBOL	MM		
	MIN	NOM	MAX		MIN	NOM	MAX
*A	4.80	5.00	5.20	F1	5.70	5.80	5.90
A1	1.90	2.00	2.10	F2	4.85	5.00	5.15
*b	1.10	1.20	1.30	*e	5.39	5.44	5.49
b1	2.90	3.00	3.10	*L	19.72	19.92	20.12
b2	1.95	2.00	2.05	*L1	4.03	4.13	4.23
*B1	3.00	3.10	3.20	θ1	5°	7°	9°
*B2	2.00	2.10	2.20	θ2	1°	2°	3°
*c	0.50	0.6	0.70	θ3	13°	15°	17°
*D	20.80	21	21.20	*ΦP1	3.50	3.60	3.70
D1	16.40	16.55	16.70	ΦP2	7.09	7.19	7.29
D2	1.07	1.17	1.27	ΦP3	2.40	2.50	2.60
*E	15.60	15.80	16.00	*Q1	2.31	2.41	2.51
E1	13.11	13.26	13.41	S	6.05	6.15	6.25
E2	2.40	2.50	2.60	R	0.30	0.40	0.50
E3	6.10	6.20	6.30	带*为关键检验尺寸			

注:
1.表面粗糙度 Ra =1.14±0.20um
2. 带*为关键检验尺寸

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