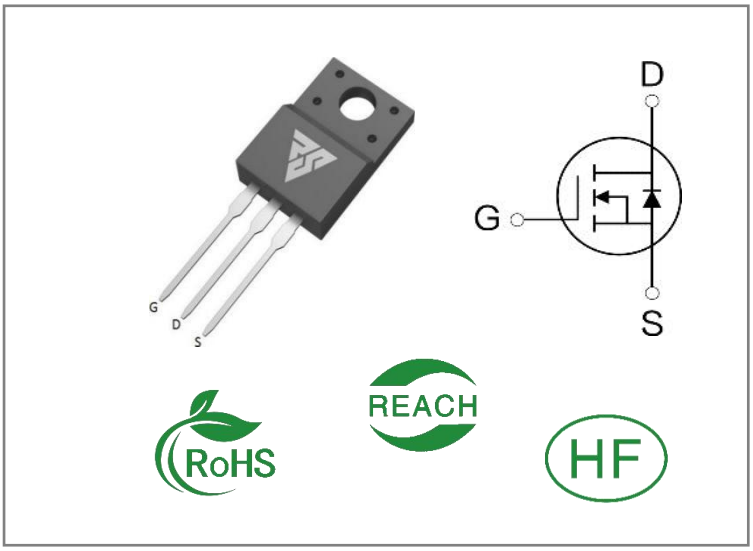
ID	R_{DS}(ON)(Typ)	VDSS
10A	0.78Ω	650V



Applications:

- High efficiency mode power supplies
- Electronic lamp ballasts
- UPS

Features:

- Low Crss
- Low gate charge
- Fast switching
- Improved ESD capability
- Improved dv/dt capability
- 100% avalanche energy test

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS10N65HF	TO-220F	RS10N65HF	Tube	50 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS10N65HF	Units
VDSS	Drain-to-Source Voltage	650	V
ID	Continuous Drain Current TC=25℃ Continuous Drain Current TC=100℃	10* 6*	A
IDM	Pulsed Drain Current (note 1)	35	
PD	Power Dissipation	50	W
PD(DF)	PowerDissipationDeratingFactor	0.4	W/℃
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy (note 2)	500	mJ
IAR	AvalancheCurrent (note 1)	10	A
EAR	RepetitiveAvalancheEnergy (note 1)	17	mJ
dv/dt	Peak Diode Recovery (note 3)	4.5	V/ns
TL	Maximum Temperature for Soldering	300	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS10N65HF	Units	Test Conditions
RθJC	Junction-to-Case	2.5	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650	--	--	V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=650V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	0.78	0.85	Ω	VGS=10V ID=5A
VGS (TH)	Gate Threshold Voltage	2	--	4	V	VGS=VDS ID=250μA
Gfs	ForwardTransconductance (note 4)	--	8	--	S	VDS=40V ID=5A

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	42	80	nS	VDS=300V ID=10A RG=25Ω (note 4,5)
trise	Rise Time	--	24	40		
td(OFF)	Turn- OFF Delay Time	--	135	200		
tfall	Fall Time	--	45	86		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1760	2000	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	140	170		
Crss	Reverse Transfer Capacitance	--	10.9	23		
Qg	Total Gate Charge	--	45	60	nC	VDS=480V ID=10A VGS=10V (note 4,5)
Qgs	Gate- to- Source Charge	--	8	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	15	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	10	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	40	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=10A,VGS=0V
trr	Reverse Recovery Time	--	418	--	nS	VGS=0V IS=10A di/dt=100A/μs (note 4)
Qrr	Reverse Recovery Charge	--	3.4	--	μC	

Notes:

1：Pulse width limited by maximum junction temperature 2：L=10mH, IAS=10A, VDD=50V, RG=25Ω, Starting TJ=25℃

3：ISD ≤10A, di/dt ≤300A/μs, VDD≤BVDSS, Starting TJ=25℃

4：Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%

5：Essentially independent of operating temperature

Typical Feature Curve

Fig. 1 On-State Characteristics

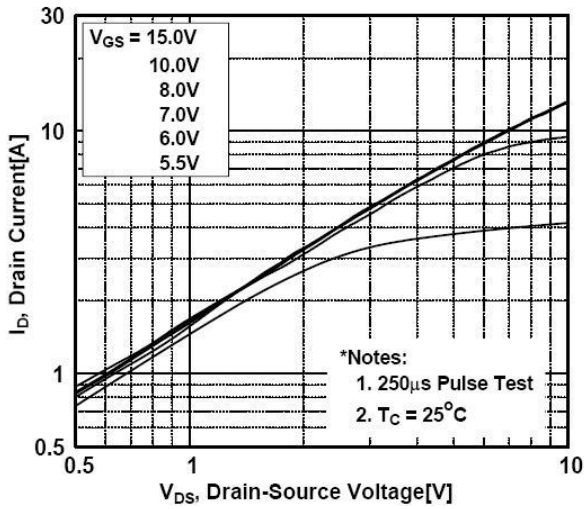


Fig. 2 Transfer Characteristics

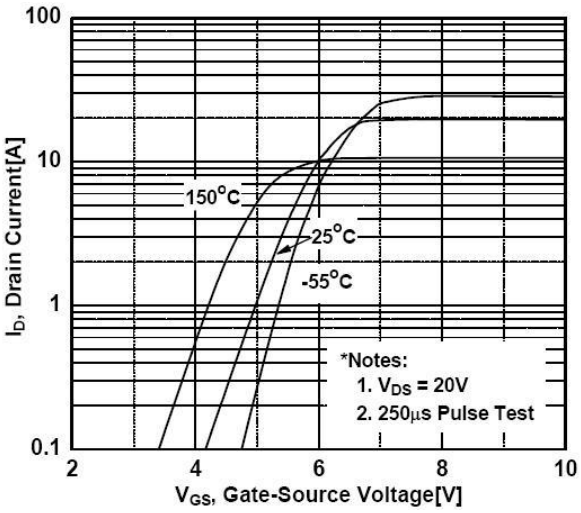


Fig.3 Breakdown Voltage Variation vs Temperature

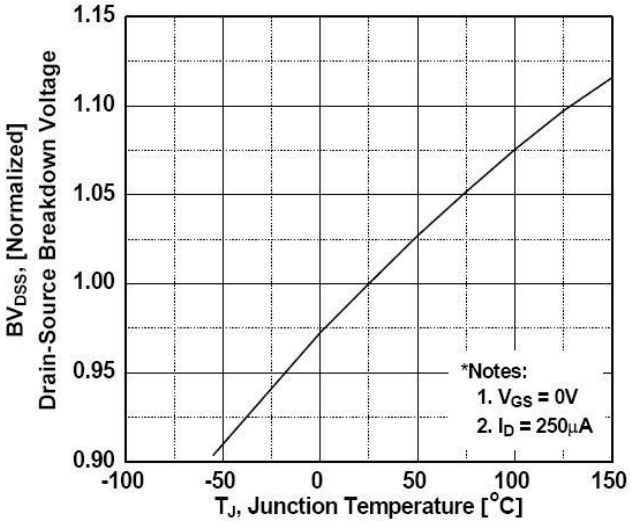


Fig. 4 On-Resistance Variation vs Temperature

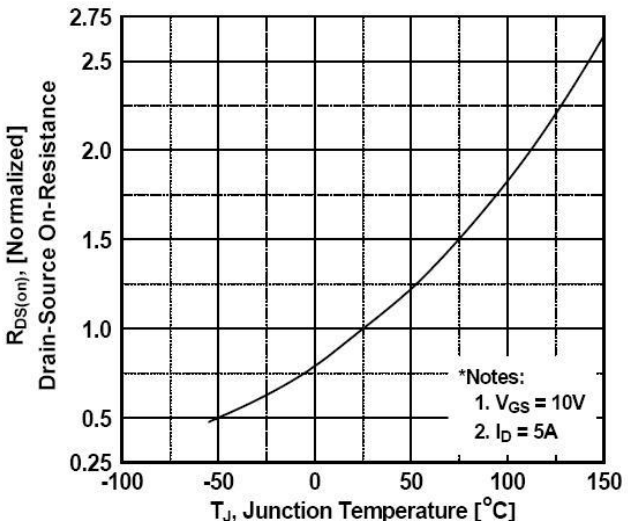


Fig. 5 Capacitance Characteristics

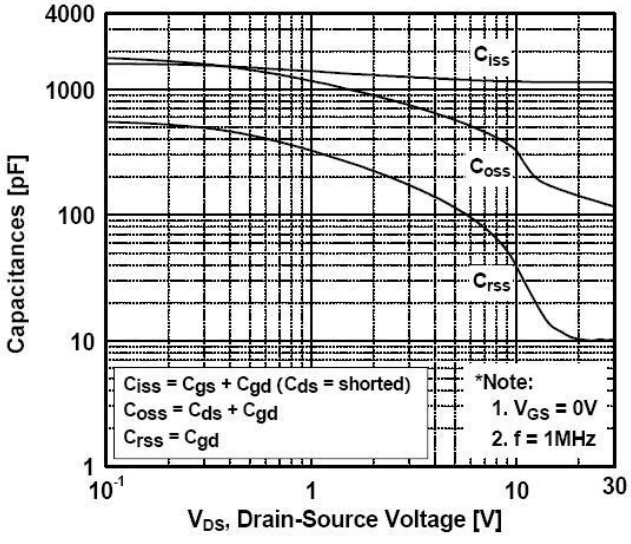
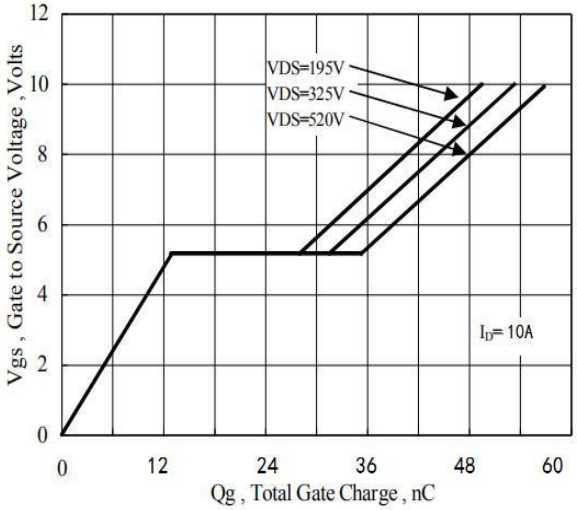


Fig. 6 Gate Charge Characteristics



Typical Feature Curve

Fig.7 Maximum Safe Operating Area

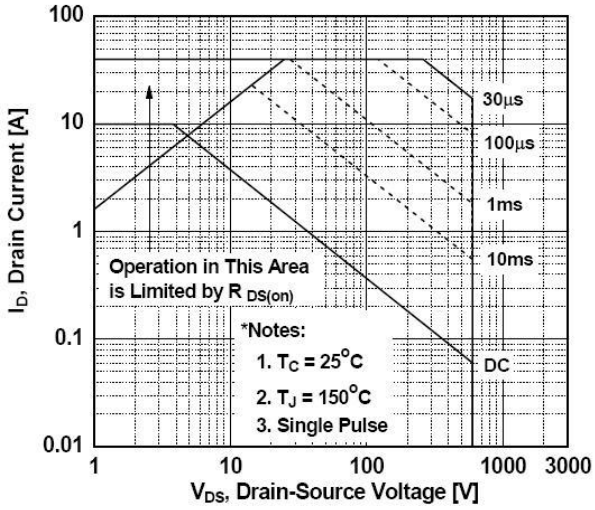


Fig. 8 Maximum Drain Current vs Case Temperature

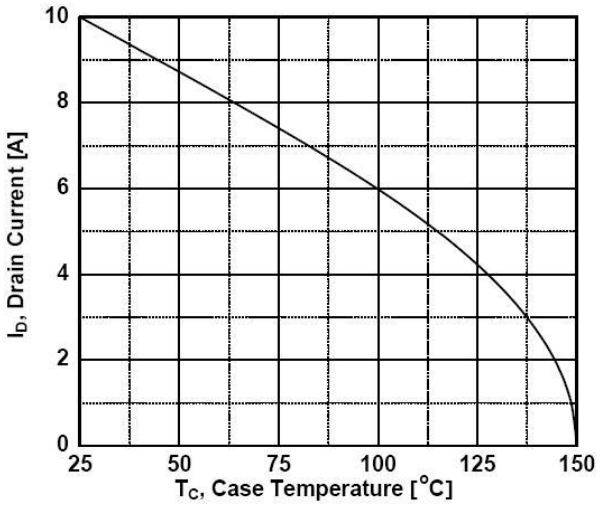
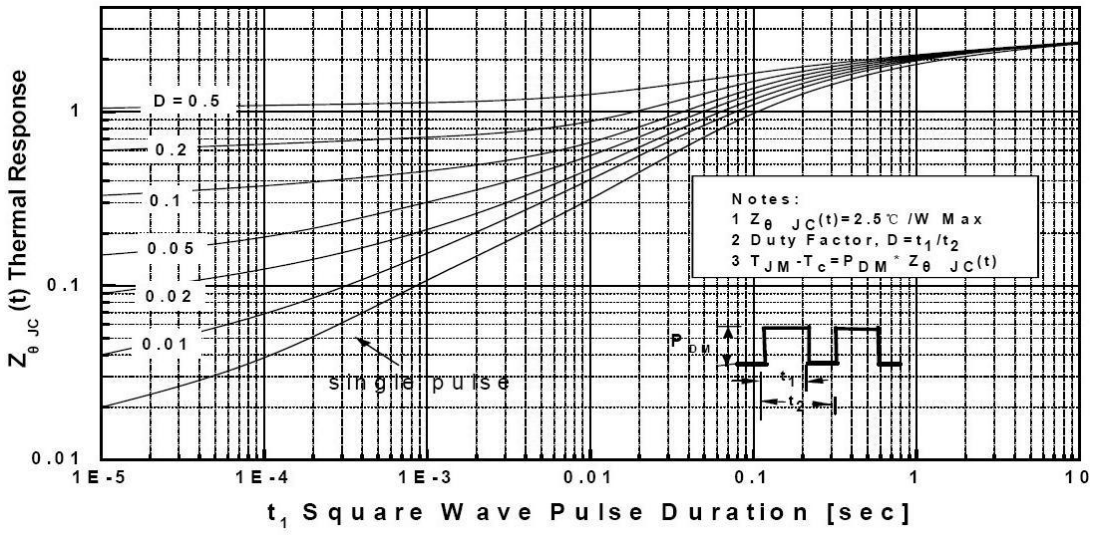
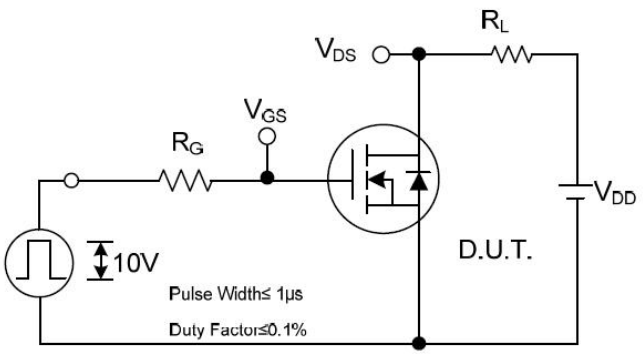
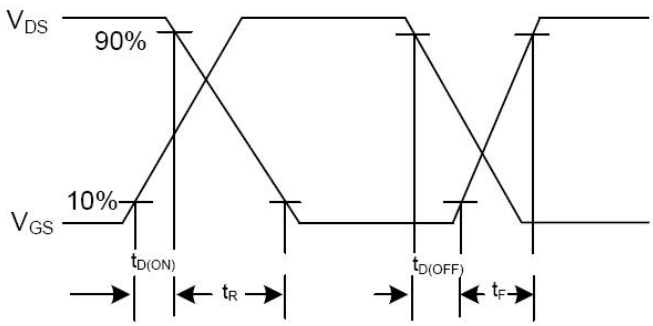


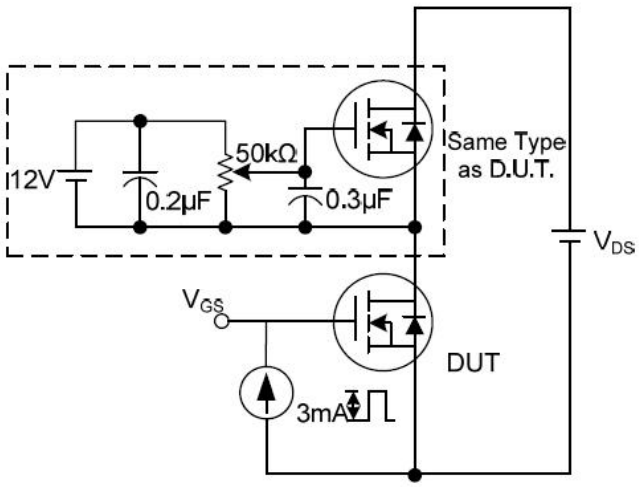
Fig. 9 Transient Thermal Response Curve

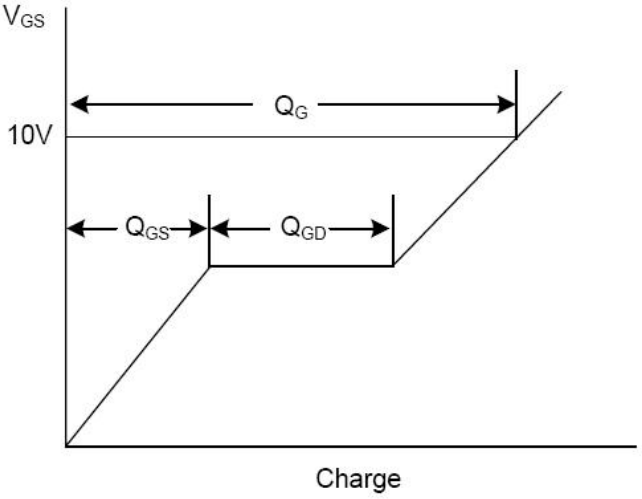


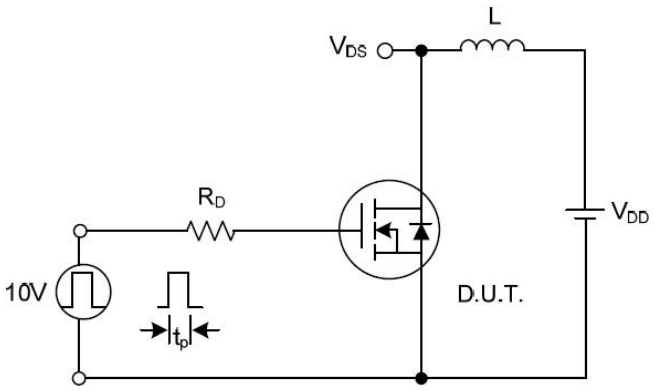
Test Circuits and Waveforms

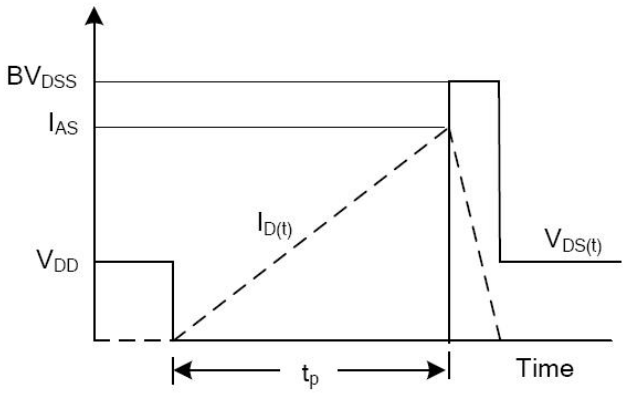




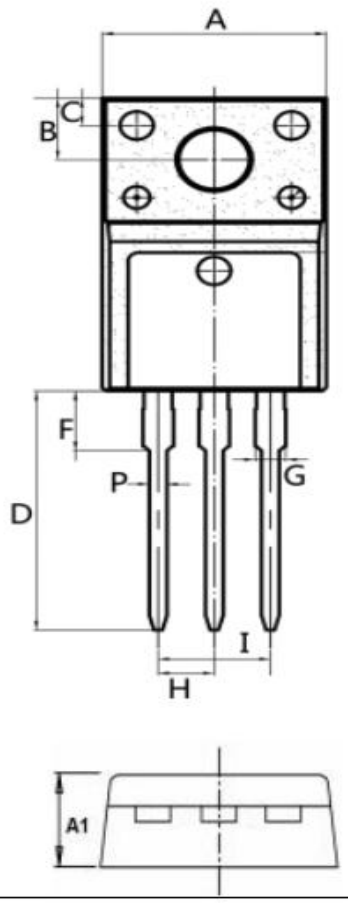








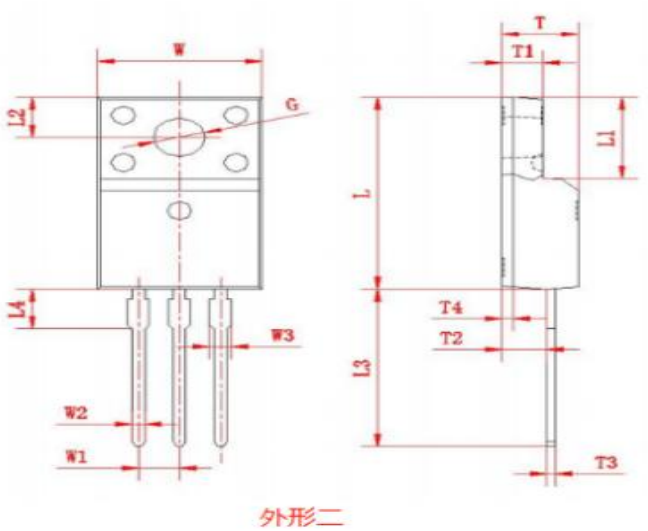
Package outline drawing(TO-220F Unit: mm)



外形一

Dim.	Min.	Max.
A	9.95	10.36
A1	4.5	5.0
B	2.95	3.25
C	1.25	1.45
D	12.60	13.60
E	0.40	0.60
F	2.8	3.5
G	1.30	1.45
H	(2.54)	
I	(5.08)	
J	4.60	4.75
K	2.45	2.65
L	6.5	6.8
M	15.4	16.0
N	2.25	3.05
O	0.45	0.55
P	0.70	0.90

All Dimensions in millimeter



外形二

Dim.	Min.	Max.
W	9.95	10.36
W1	(2.54)	
W2	0.70	0.90
W3	1.25	1.47
L	15.67	16.07
L1	6.48	6.88
L2	3.2	3.4
L3	12.6	13.6
L4	(3.23)	
T	4.50	4.90
T1	2.34	2.74
T2	2.25	2.95
T3	0.45	0.60
T4	(0.70)	
G	3.08	3.28

All Dimensions in millimeter

Disclaimers:

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights,nor the rights of others.Reproduction of inform- ation in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as cri- tical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.
As used herein:
1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,
c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.