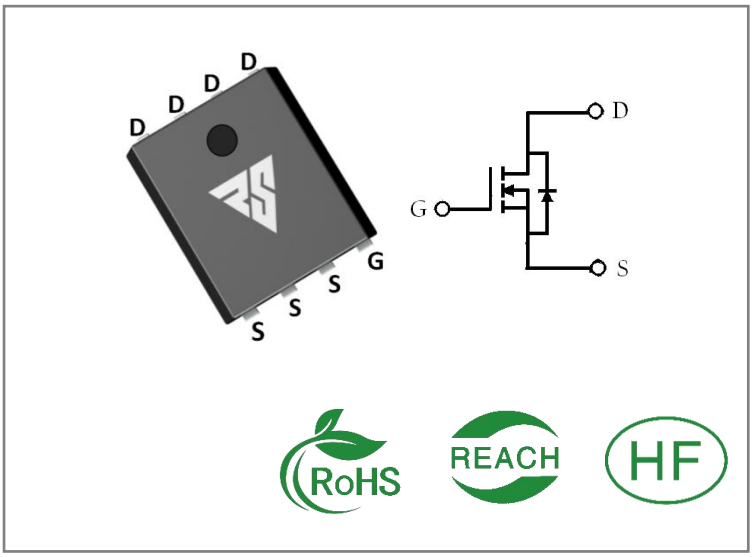
ID	R_{DS}(ON)(Typ)	VDSS
55A	7mΩ	30V



Applications:
- Load Switch
- PWM Applications
- Power Managment

Features:
- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced Trench technology

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS30N55G	PDFN5*6	RS30N55G	Tape&reel	2500 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS30N55G	Units
VDSS	Drain-to-Source Voltage	30	V
ID	Continuous Drain Current TC=25℃ (Note 1)	55	A
ID	Continuous Drain Current TC=100℃ (Note 1)	35	
IDM	Pulsed Drain Current (Note 2)	220	
PD	Power Dissipation TC=25℃ (Note 3)	53.6	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH, VDD =20V, VGS=10V,IAS=17A	72	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature
Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS30N55G	Units	Test Conditions
RθJC	Junction-to-Case (Note 1)	2.8	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	30	--	--	V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=30V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance （Note 2）	--	7	8.4	mΩ	VGS=10V ID=20A
		--	10	13	mΩ	VGS=4.5V ID=10A
VGS (TH)	Gate Threshold Voltage	1.0	1.5	2.5	V	VGS=VDS ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	5	--	nS	VDS=15V VGS=10V ID=10A RG=2Ω
trise	Rise Time	--	9.5	--		
td(OFF)	Turn- OFF Delay Time	--	28	--		
tfall	Fall Time	--	8	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1148	--	pF	VGS=0V VDS=15V f=1.0MHz
Coss	Output Capacitance	--	120	--		
Crss	Reverse Transfer Capacitance	--	104	--		
RG	Gate Resistance	--	1.6	--	Ω	VGS=0V VDS=0V f=1.0MHz
Qg	Total Gate Charge	--	24.4	--	nC	VDS=15V ID=10A VGS=10V
Qgs	Gate- to- Source Charge	--	2.9	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	5.0	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	55	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	220	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=20A VGS=0V
trr	Reverse Recovery Time	--	10	--	nS	Tj=25℃ IF=10A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	2.6	--	nC	

Notes:

* 1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
* 3. The power dissipation is limited by 175℃ junction temperature.
* 4.The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

Typical Feature Curve

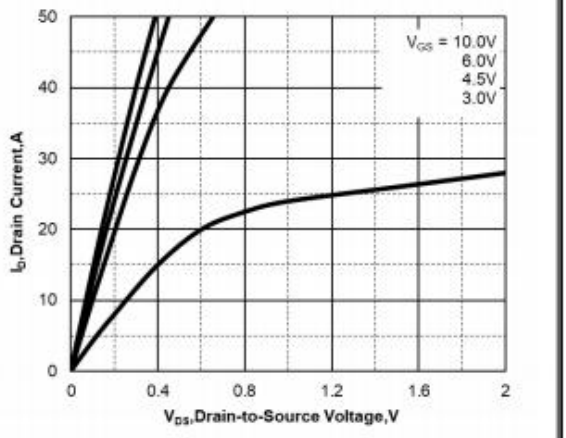


Fig1: Typical Output Characteristics

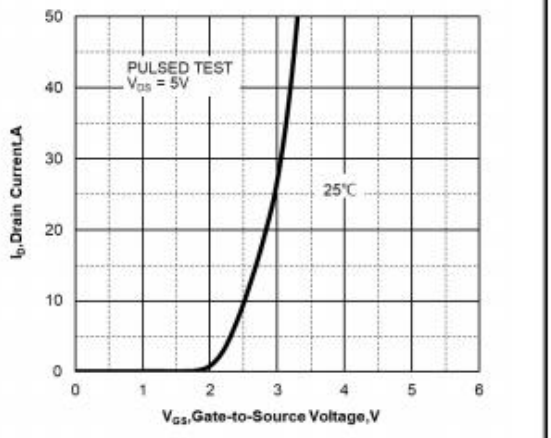


Fig 2: Typical Transfer Characteristics

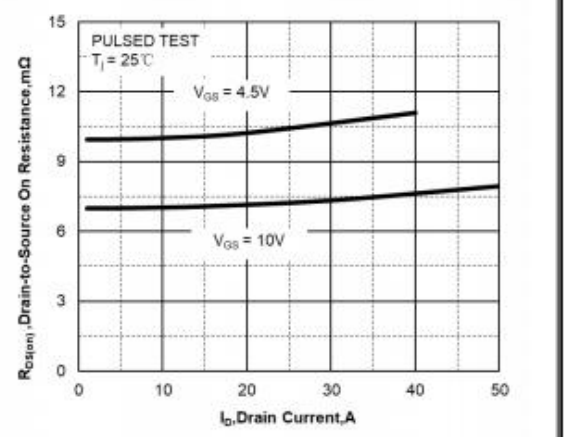


Fig 3: On-Resistance VS. Drain Current

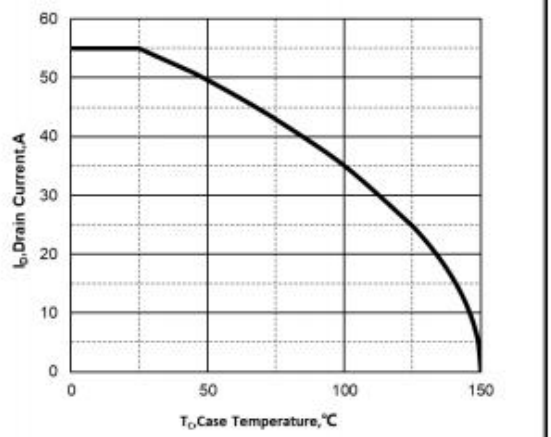


Fig 4: Maximum Continuous Drain Current VS. Case Temperature

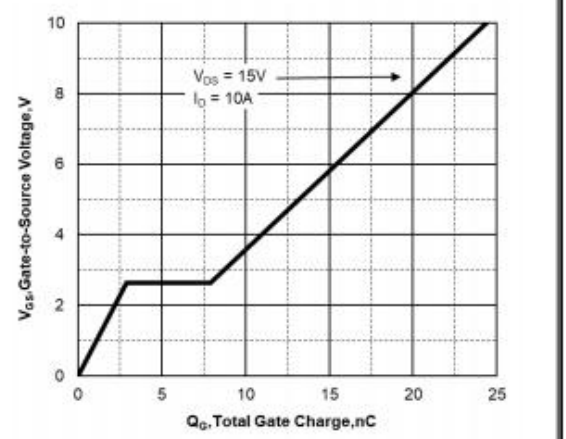


Fig 5: Gate Charge Characteristics

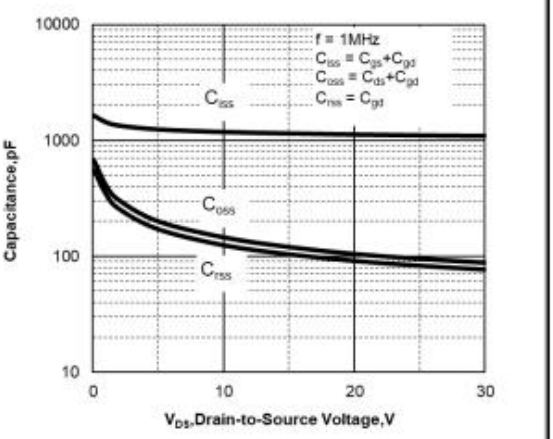


Fig 6: Capacitance Characteristics

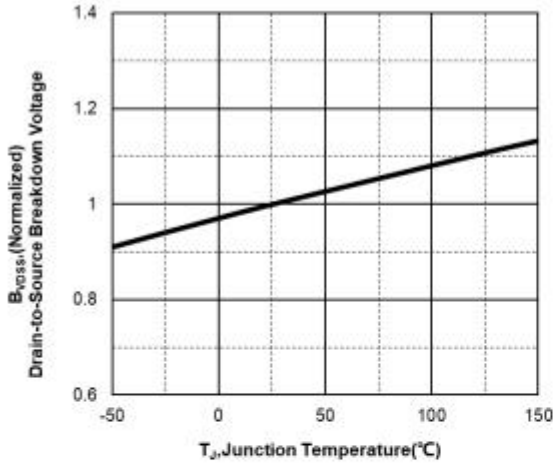


Fig 7: Normalized Breakdown Voltage VS. Junction Temperature

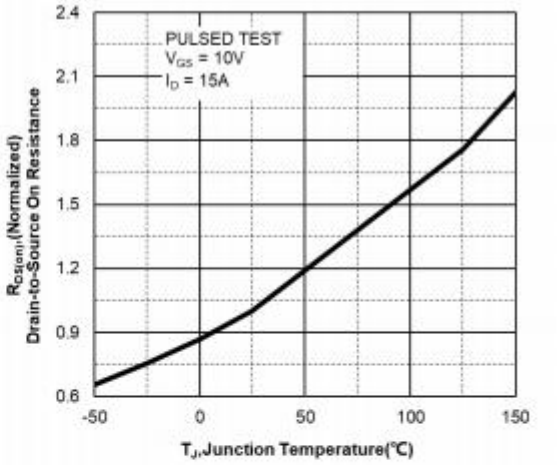


Fig 8: Normalized on Resistance VS. Junction Temperature

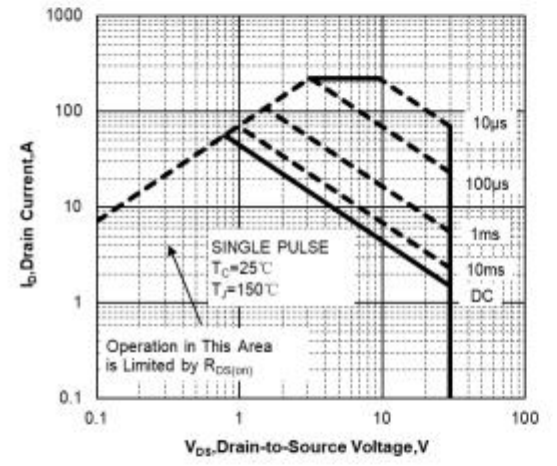


Fig 9: Maximum Safe Operating Area

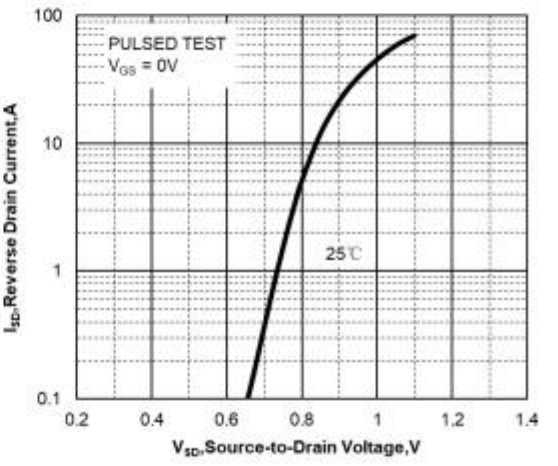


Fig 10: Body Diode Forward Characteristics

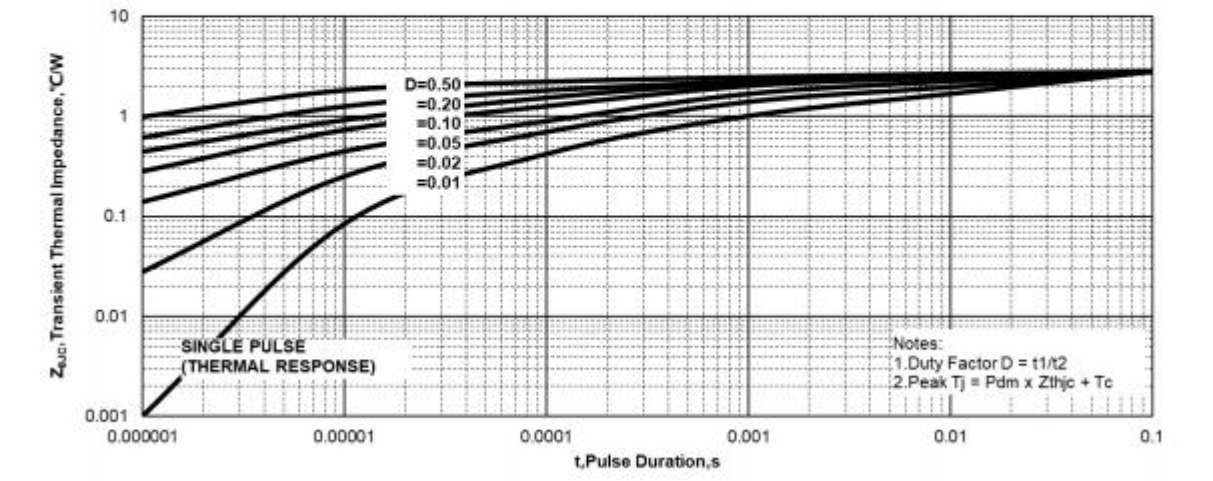
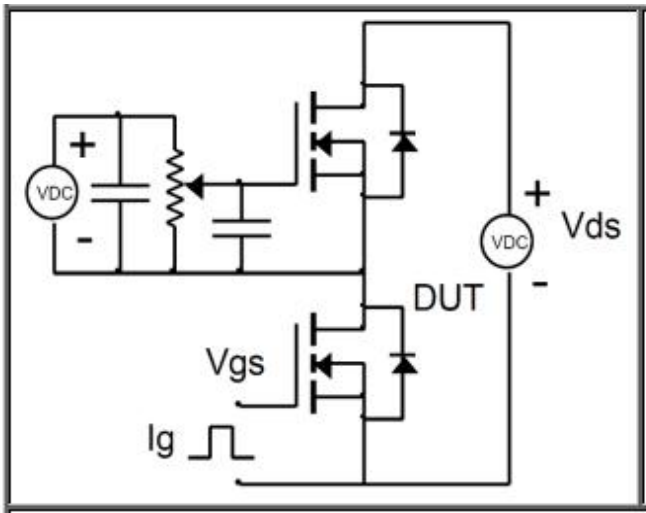


Fig.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test Circuits and Waveforms



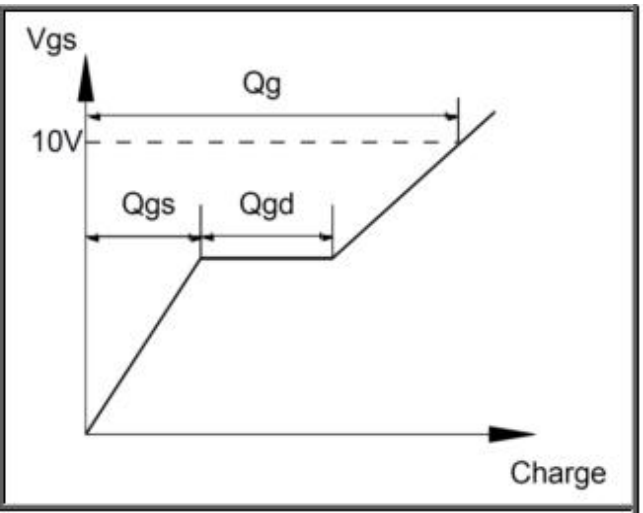
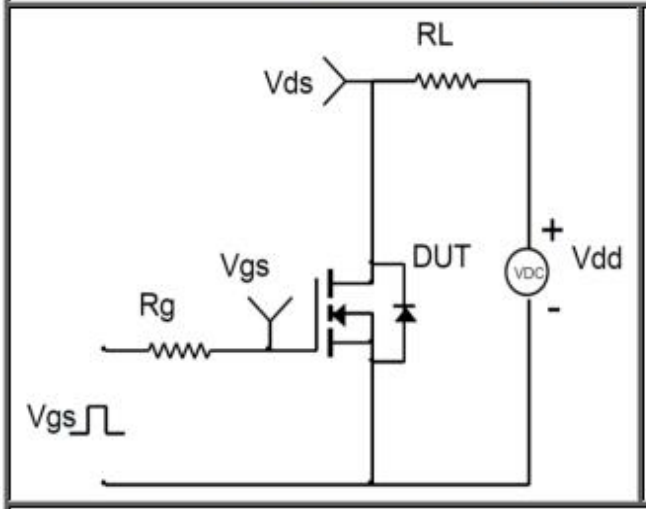


Fig 12: Gate Charge Test Circuit and Waveforms



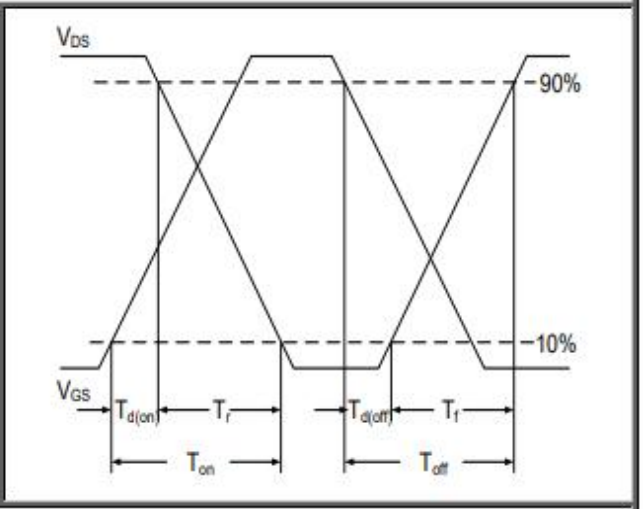
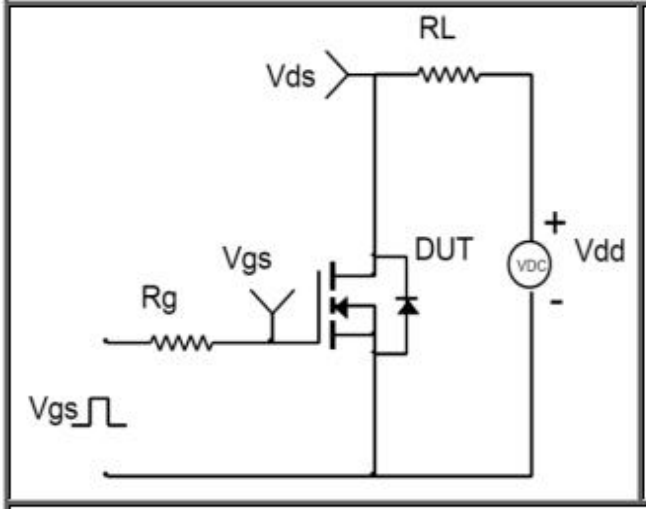


Fig 13: Resistive Switching Test Circuit and Waveforms



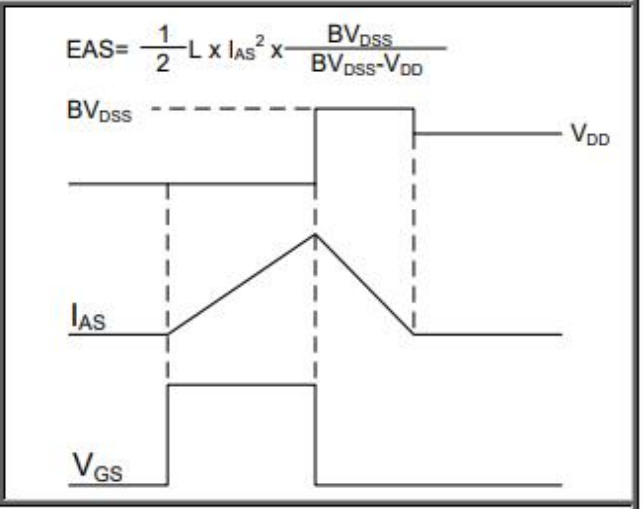
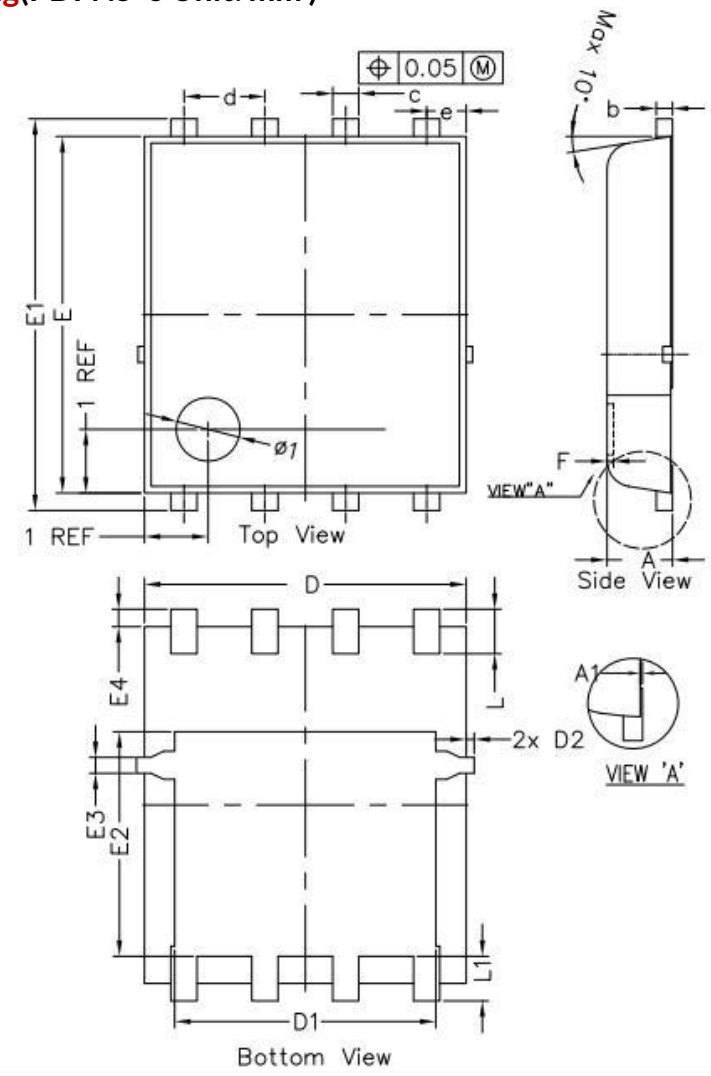


Fig 14: Unclamped Inductive Switching Test Circuit and Waveforms

Package outline drawing(PDFN5*6 Unit: mm)



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
* A	0.900	1.000	1.100	0.035	0.039	0.043
A1	0.000	---	0.050	0.000	----	0.002
b	0.246	0.254	0.312	0.010	0.010	0.012
* c	0.310	0.410	0.510	0.012	0.016	0.020
d		1.27 BSC			0.050 BSC	
* D	4.950	5.050	5.150	0.195	0.199	0.203
D1	4.000	4.100	4.200	0.157	0.161	0.165
⚠ * D2	---	---	0.125	---	---	0.005
e		0.62 BSC			0.024 BSC	
* E	5.500	5.600	5.700	0.217	0.220	0.224
* E1	6.050	6.150	6.250	0.238	0.242	0.246
E2	3.425	3.525	3.625	0.135	0.139	0.143
E3	0.150	0.250	0.350	0.006	0.010	0.014
* E4	0.175	0.275	0.375	0.007	0.011	0.015
F	-	-	0.100	-	-	0.004
⚠ * L	0.500	0.600	0.700	0.02	0.02	0.03
L1	0.600	0.700	0.800	0.02	0.03	0.03

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