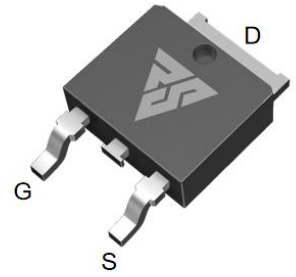
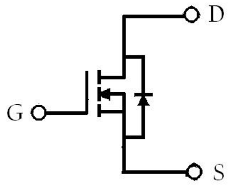
ID	R_{DS}(ON)(Typ)	VDSS
190A	1.8mΩ	30V





Applications:

- Load Switch
- PWM Applications
- Power Managment

Features:

- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced Trench technology

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS30N190D	T0-252	RS30N190D	Tape&reel	2500 PCS

Absolute Maximun Ratings **Tc= 2 5℃ unless otherwise specified**

Symbol	Parameter	RS30N190D	Units
VDSS	Drain-to-Source Voltage	30	V
ID	Continuous Drain Current TC=25℃ （Note 1）	190	A
ID	Continuous Drain Current TC=100℃ （Note 1）	122	
IDM	Pulsed Drain Current （Note 2）	760	
PD	Power Dissipation TC=25℃ （Note 3）	176	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH, VDD =20V, VGS=10V,IAS=51A	650	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS30N190D	Units	Test Conditions
RθJC	Junction-to-Case （Note 1）	0.80	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of +150℃

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	30	--	--	V	VGS=0V ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=30V VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance （Note 2）	--	1.8	2.2	mΩ	VGS=10V ID=30A
		--	2.6	3.3	mΩ	VGS=4.5V ID=20A
VGS (TH)	Gate Threshold Voltage	1.0	1.7	2.5	V	VGS=VDS ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	26	--	nS	VDS=15V VGS=10V ID=30A RG=3Ω
trise	Rise Time	--	20	--		
td(OFF)	Turn- OFF Delay Time	--	88	--		
tfall	Fall Time	--	19	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	7281	--	pF	VGS=0V VDS=15V f=1.0MHz
Coss	Output Capacitance	--	897	--		
Crss	Reverse Transfer Capacitance	--	806	--		
RG	Gate Resistance	--	0.7	--	Ω	VDS=0V VGS=0V f=1.0MHz
Qg	Total Gate Charge	--	151	--	nC	VDS=15V ID=30A VGS=10V
Qgs	Gate- to- Source Charge	--	19.7	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	30.2	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.		Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--		--	190	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--		--	760	A	
VSD	Diode Forward Voltage	--		--	1.2	V	IS=30A VGS=0V
trr	Reverse Recovery Time	--		39	--	nS	VGS=0V IS=30A di/dt=100A/µs
Qrr	Reverse Recovery Charge	--		45	--	nC	
ton	Forward Turn-on Time		Intrinsic turn-on time is negligible (turn-on is dominated by LS +LD)				

Notes:

* 1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
* 2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%.
* 3. The power dissipation is limited by 175℃ junction temperature.
* 4.The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

Typical Feature Curve

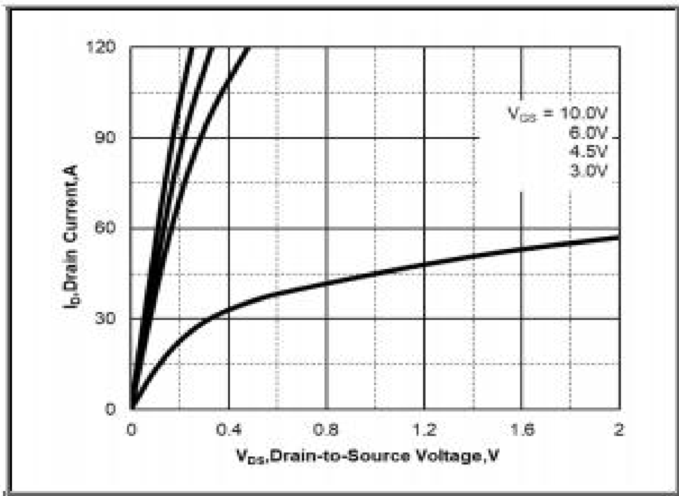


Fig1: Typical Output Characteristics

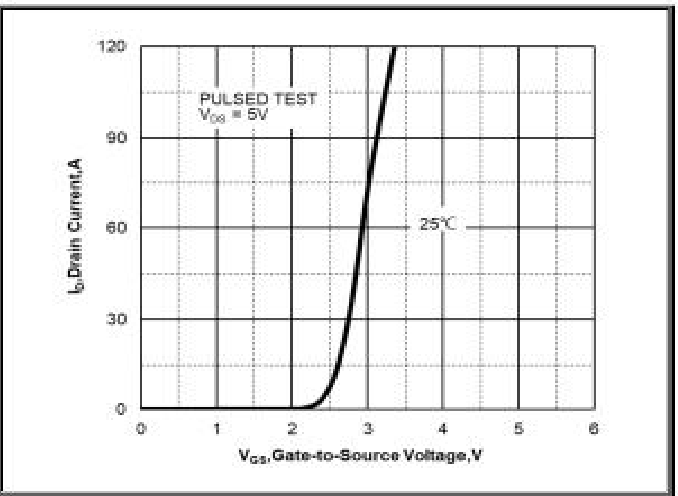


Fig 2: Typical Transfer Characteristics

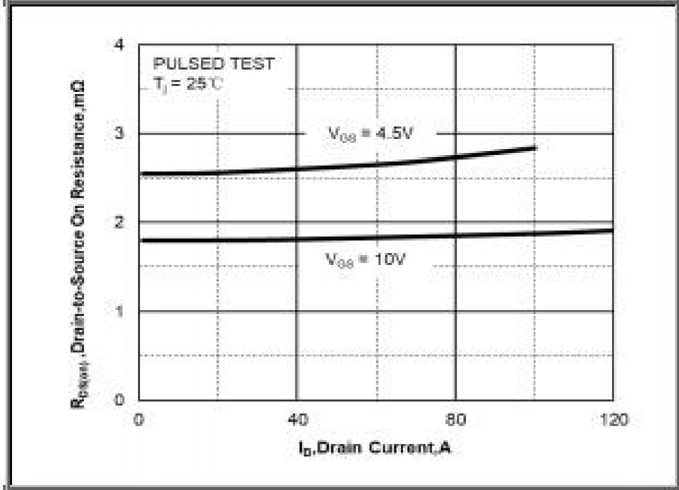


Fig 3: On-Resistance VS. Drain Current

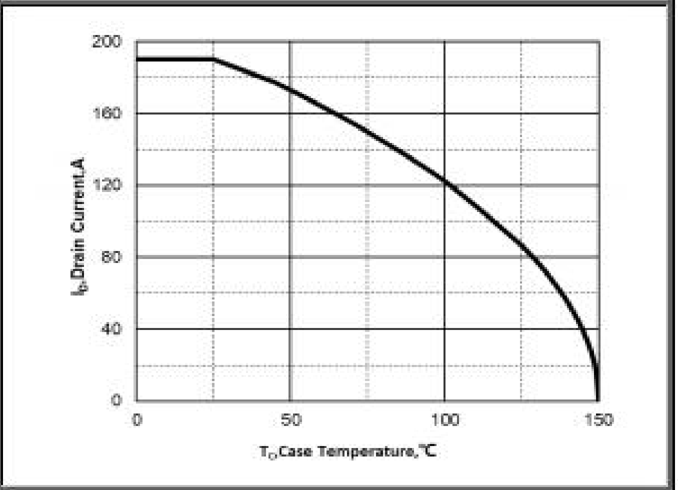


Fig 4: Maximum Continuous Drain Current VS. Case Temperature

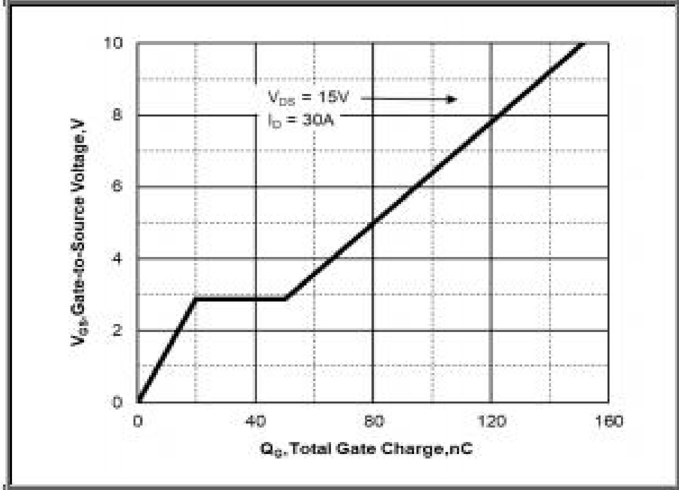


Fig 5: Gate Charge Characteristics

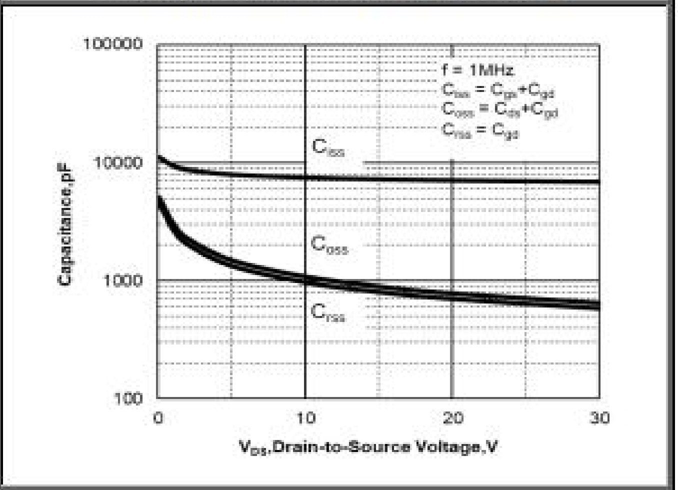


Fig 6: Capacitance Characteristics

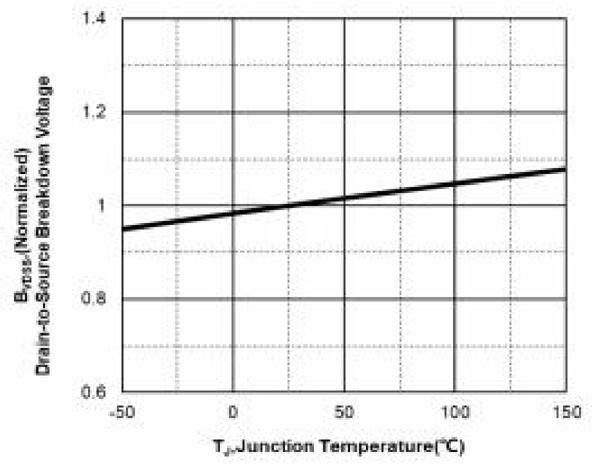


Fig 7: Normalized Breakdown Voltage VS. Junction Temperature

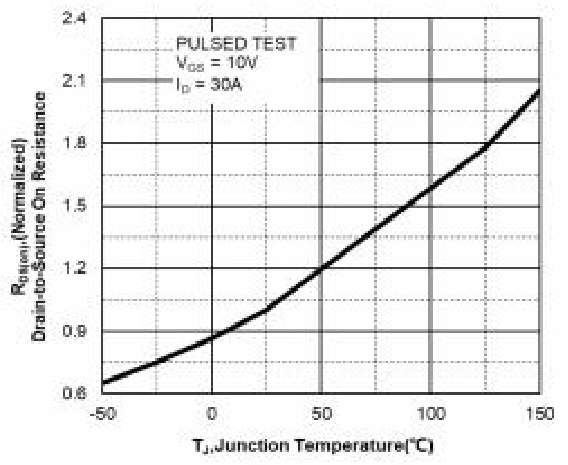


Fig 8: Normalized on Resistance VS. Junction Temperature

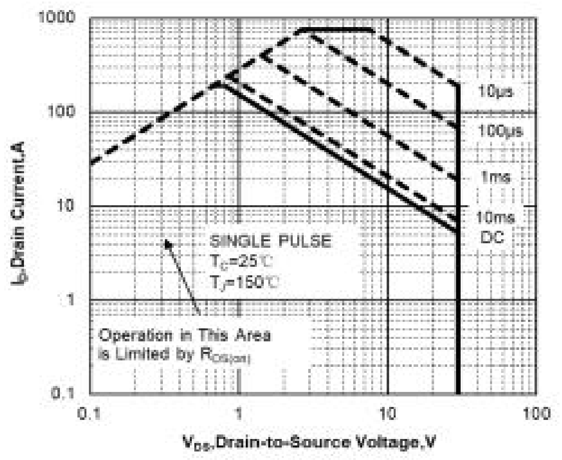


Fig 9: Maximum Safe Operating Area

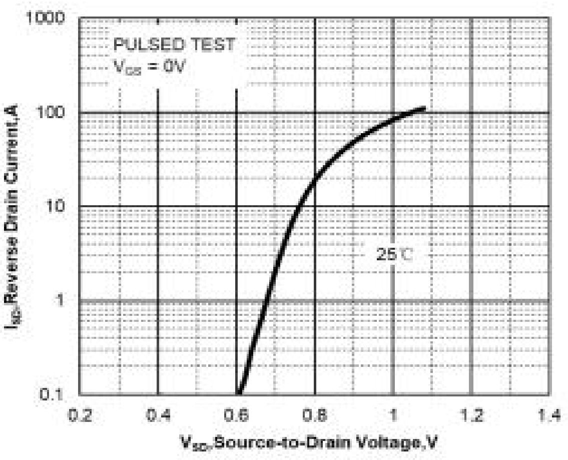


Fig 10: Body Diode Forward Characteristics

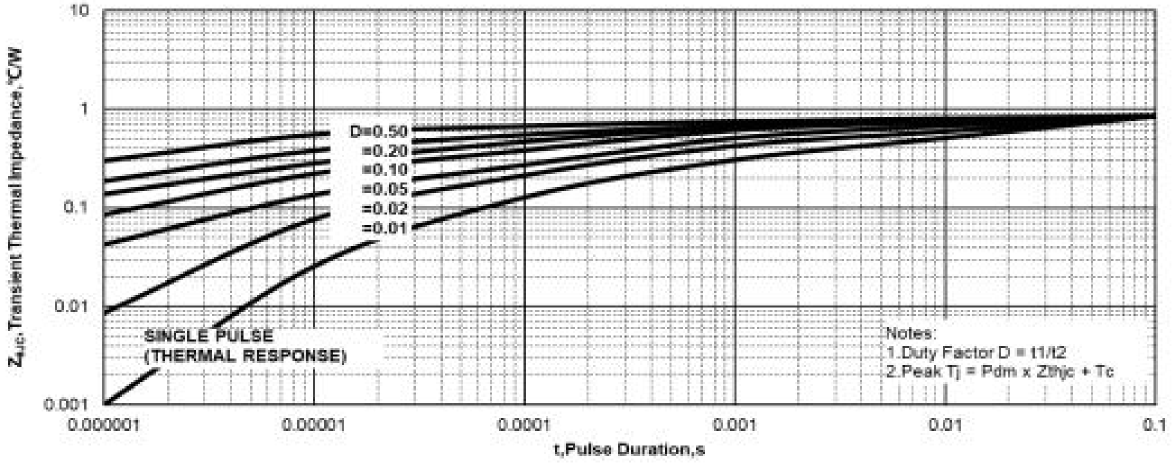


Fig.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test Circuits and Waveforms

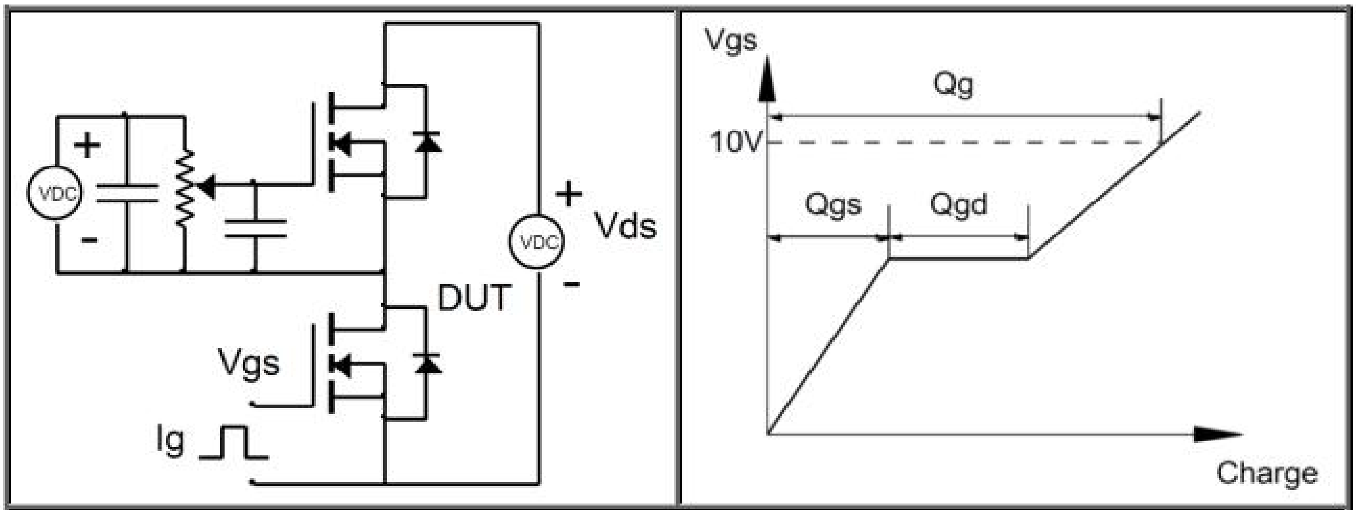


Fig 12: Gate Charge Test Circuit and Waveforms

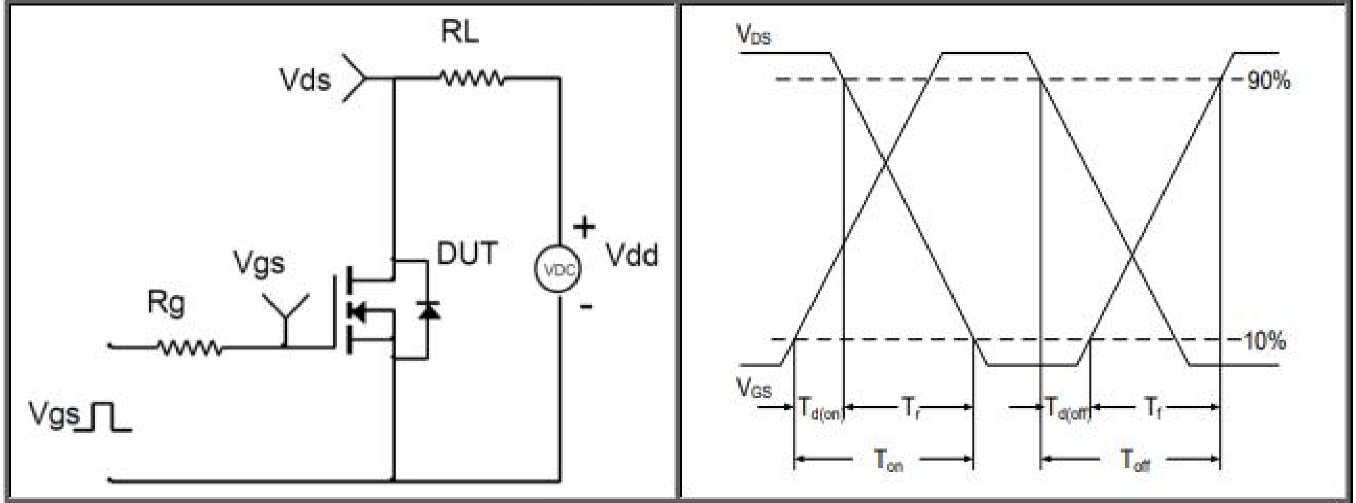


Fig 13: Resistive Switching Test Circuit and Waveforms

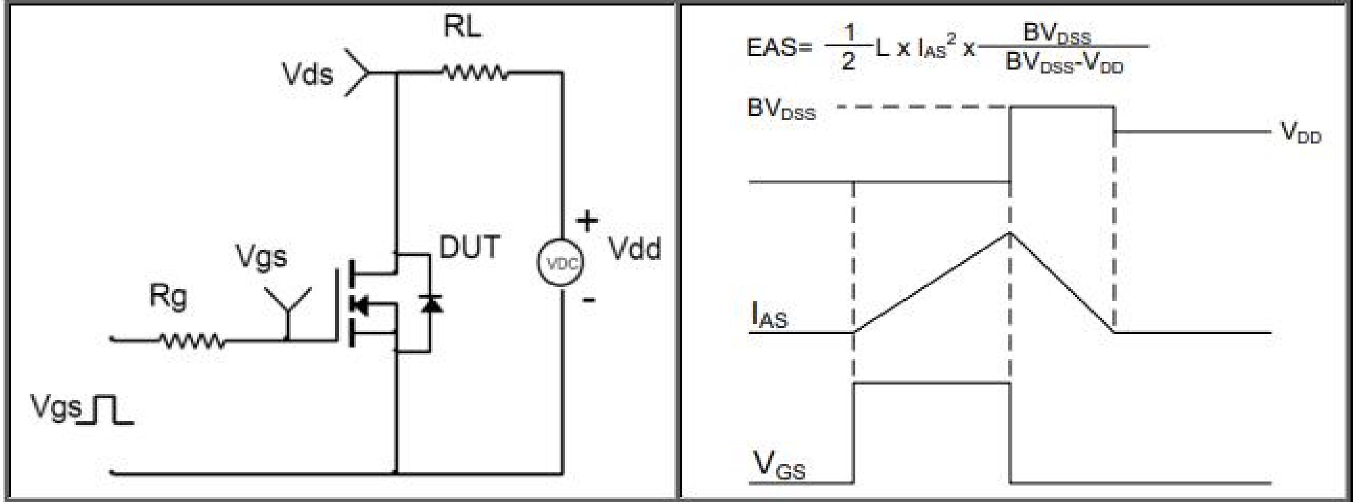
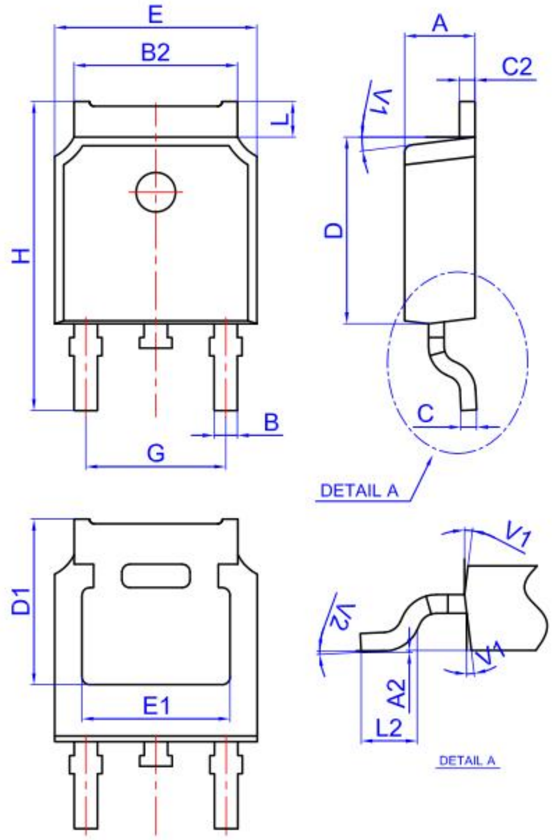


Fig 14: Unclamped Inductive Switching Test Circuit and Waveforms

Package outline drawing(TO-252 Unit: mm)



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

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